


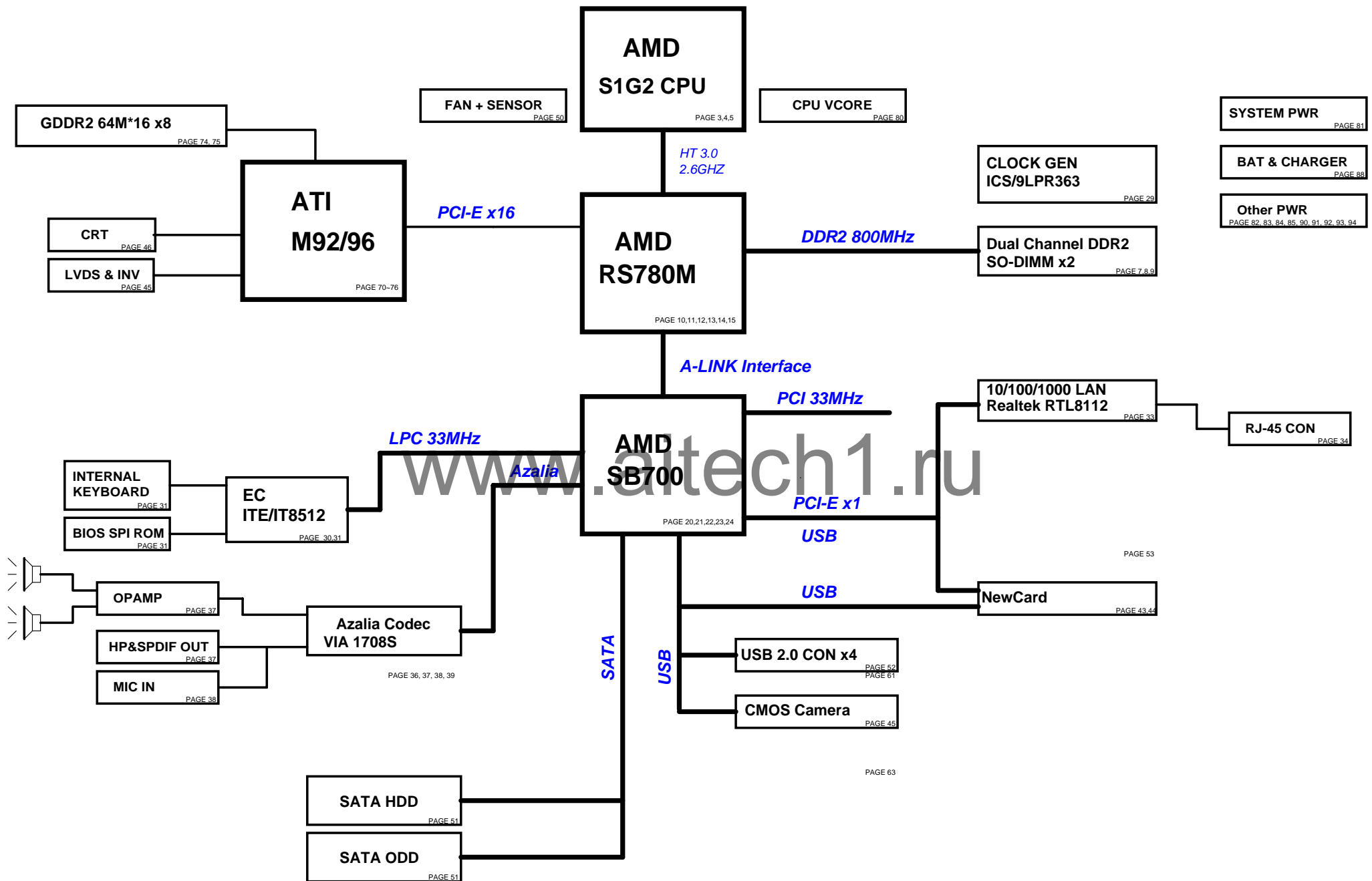
[illegible]

# K40AA SCHEMATIC R10

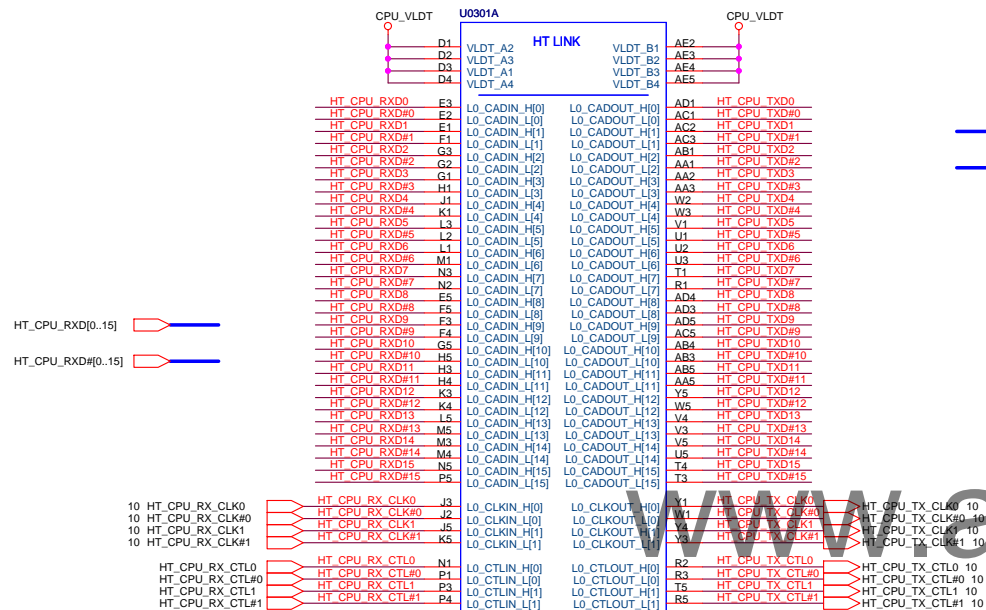
PAGE	Content	PAGE	Content
SYSTEM PAGE REF.			
3	SCHEMATIC INFORMATION	58	ROBSON
4	CPU-PENRYN(1)	60	DC & BAT IN
5	CPU-PENRYN(2)	61	BLUE TOOTH
6	CPU CAP	62	TPM & CAP sensor
7	DDR2 SO-DIMM_0	63	Finger Print
8	DDR2 SO-DIMM_1	65	SCREW HOLE & NUT & SPRING
9	DDR2 ADDRESS TERMINATION	66	E-SATA
10	NB_-CANTIGA--CPU (1)	69	History
11	NB_-CANTIGA--DDR2/PEG (2)	70	VGA_nVIDIA_NB9X_PCIE
12	NB_-CANTIGA--DDR2 bus (3)	71	VGA_nVIDIA_NB9X_FB
13	NB_-CANTIGA--POWER (4)	72	VGA_nVIDIA_NB9X_Display
14	NB_CANTIGA--POWER (5)	73	VGA_nVIDIA_NB9X_XTAL/Other
15	NB_-CANTIGA--GND/Strapping (6)	74	VGA_nVIDIA_NB9MGS_PCIE
20	SB_-ICH9M--(1)-SATA,AUDIO,ACZ	75	VGA_nVIDIA_NB9X_GPIO
21	SB_-ICH9M--(2)-PCI,PCI-E,USB	76	VGA_nVIDIA_NB9X_VRAM
22	SB_-ICH9M--(3)-GPIO	77	VGA_nVIDIA_NB9X_VRAM
23	SB_-ICH9M--(4)-PWR/GND		
24	SB_-ICH9M--Other		
25	SPI ROM		
29	CLK-ICS9LPR363DGLF-T		
30	EC-IT8512 (1)		
31	EC-IT8512 (2)		
32	POWER-ON SEQUENCE		
33	PCI-E LAN_RTL8111C		
34	RJ45		
35	MDC		
36	CODEC-ALC663		
37	AUDIO_AMP-1431&HP		
38	Microphone&Line-in		
40	CARDBUS R5C833(PCI I/F)		
41	CARDBUS R5C833(1394 & SD)		
42	7 in 1 CARD READER		
43	EXPRESS CARD		
44	Debug		
45	LVDS&INVERTER CONNECTOR		
46	CRT		
48	HDMI		
50	Thermal Sensor		
51	HDD & CDROM		
52	USB Port X3		
53	WLAN(MINI CARD)		
56	LED & SW		
57	DISCHARGE		
POWER PAGE REF.			
		80_POWER_VCORE	
		81_POWER_SYSTEM	
		82_POWER_I/O_1.5VS & 1.05VS	
		83_POWER_I/O_DDR & VTT	
		85_POWER_VGA_CORE & +1.1VO	
		87_POWER_SHUTDOWN#	
		88_POWER_CHARGER	
		90_POWER_PROTECT	
		91_POWER_LOAD SWITCH	
		92_POWER_PROTECT	
		93_POWER_SIGNAL	
		94_POWER_FLOWCHART	

		Title : Page Reference	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	K40AA		1.00
Date: Monday, February 09, 2009		Sheet	1 of 87

## K40AA Block Diagram



1.5A

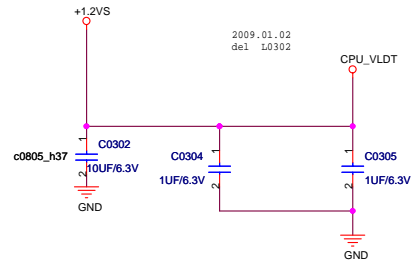


SOCKET638

Change P/N to 12G011306380

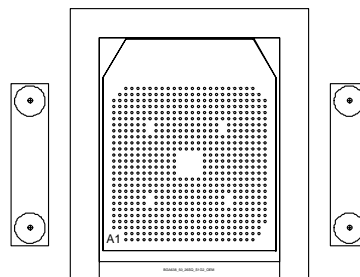
071113

Do not cross plane.

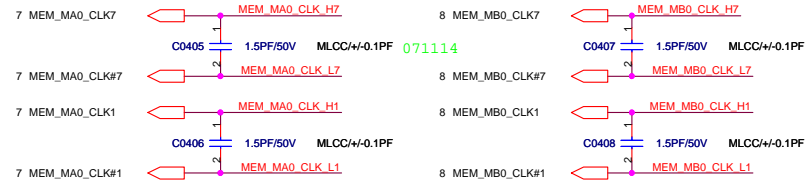


Place close to socket

\* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



place close to PROCESSOR within 1.5 inch



8 MEM\_MB\_DATA0[0..63]

MEM\_MB\_DATA0 C11

MEM\_MB\_DATA1 A11

MEM\_MB\_DATA2 A14

MEM\_MB\_DATA3 B14

MEM\_MB\_DATA4 G11

MEM\_MB\_DATA5 E11

MEM\_MB\_DATA6 D12

MEM\_MB\_DATA7 A13

MEM\_MB\_DATA8 A15

MEM\_MB\_DATA9 A16

MEM\_MB\_DATA10 A18

MEM\_MB\_DATA11 A20

MEM\_MB\_DATA12 C14

MEM\_MB\_DATA13 D14

MEM\_MB\_DATA14 C18

MEM\_MB\_DATA15 D18

MEM\_MB\_DATA16 D20

MEM\_MB\_DATA17 A21

MEM\_MB\_DATA18 D24

MEM\_MB\_DATA19 C25

MEM\_MB\_DATA20 B20

MEM\_MB\_DATA21 C20

MEM\_MB\_DATA22 B24

MEM\_MB\_DATA23 C24

MEM\_MB\_DATA24 E23

MEM\_MB\_DATA25 E24

MEM\_MB\_DATA26 C25

MEM\_MB\_DATA27 G26

MEM\_MB\_DATA28 C26

MEM\_MB\_DATA29 D26

MEM\_MB\_DATA30 G23

MEM\_MB\_DATA31 G22

MEM\_MB\_DATA32 A24

MEM\_MB\_DATA33 A23

MEM\_MB\_DATA34 A24

MEM\_MB\_DATA35 A22

MEM\_MB\_DATA36 A26

MEM\_MB\_DATA37 A25

MEM\_MB\_DATA38 A26

MEM\_MB\_DATA39 A22

MEM\_MB\_DATA40 A22

MEM\_MB\_DATA41 A22

MEM\_MB\_DATA42 A20

MEM\_MB\_DATA43 A20

MEM\_MB\_DATA44 A24

MEM\_MB\_DATA45 A23

MEM\_MB\_DATA46 A20

MEM\_MB\_DATA47 A20

MEM\_MB\_DATA48 A21

MEM\_MB\_DATA49 A18

MEM\_MB\_DATA50 A14

MEM\_MB\_DATA51 A14

MEM\_MB\_DATA52 A19

MEM\_MB\_DATA53 A18

MEM\_MB\_DATA54 A16

MEM\_MB\_DATA55 A15

MEM\_MB\_DATA56 A13

MEM\_MB\_DATA57 A12

MEM\_MB\_DATA58 A11

MEM\_MB\_DATA59 Y11

MEM\_MB\_DATA60 A14

MEM\_MB\_DATA61 A14

MEM\_MB\_DATA62 A11

MEM\_MB\_DATA63 A11

MEM\_MB\_DM0 A12

MEM\_MB\_DM1 B16

MEM\_MB\_DM2 A22

MEM\_MB\_DM3 E25

MEM\_MB\_DM4 A26

MEM\_MB\_DM5 A22

MEM\_MB\_DM6 AC16

MEM\_MB\_DM7 AD12

MEM\_MB\_DQS0 C12

MEM\_MB\_DQS0#0 B12

MEM\_MB\_DQS1 D16

MEM\_MB\_DQS1#1 C16

MEM\_MB\_DQS2 A24

MEM\_MB\_DQS2#2 A23

MEM\_MB\_DQS3 F26

MEM\_MB\_DQS3#3 E26

MEM\_MB\_DQS4 AC25

MEM\_MB\_DQS4#4 AC26

MEM\_MB\_DQS5 AF21

MEM\_MB\_DQS5#5 AF22

MEM\_MB\_DQS6 AD16

MEM\_MB\_DQS6#6 AF12

MEM\_MB\_DQS7 AF12

MEM\_MB\_DQS7#7 AF12

MEM\_MB\_DM0 B16

MEM\_MB\_DM1 B16

MEM\_MB\_DM2 B16

MEM\_MB\_DM3 B16

MEM\_MB\_DM4 B16

MEM\_MB\_DM5 B16

MEM\_MB\_DM6 B16

MEM\_MB\_DM7 B16

MEM\_MB\_DQS0 B16

MEM\_MB\_DQS0#0 B16

MEM\_MB\_DQS1 B16

MEM\_MB\_DQS1#1 B16

MEM\_MB\_DQS2 B16

MEM\_MB\_DQS2#2 B16

MEM\_MB\_DQS3 B16

MEM\_MB\_DQS3#3 B16

MEM\_MB\_DQS4 B16

MEM\_MB\_DQS4#4 B16

MEM\_MB\_DQS5 B16

MEM\_MB\_DQS5#5 B16

MEM\_MB\_DQS6 B16

MEM\_MB\_DQS6#6 B16

MEM\_MB\_DQS7 B16

MEM\_MB\_DQS7#7 B16

MEM\_MB\_DATA0 MA\_DATA[0]

MEM\_MB\_DATA1 MA\_DATA[1]

MEM\_MB\_DATA2 MA\_DATA[2]

MEM\_MB\_DATA3 MA\_DATA[3]

MEM\_MB\_DATA4 MA\_DATA[4]

MEM\_MB\_DATA5 MA\_DATA[5]

MEM\_MB\_DATA6 MA\_DATA[6]

MEM\_MB\_DATA7 MA\_DATA[7]

MEM\_MB\_DATA8 MA\_DATA[8]

MEM\_MB\_DATA9 MA\_DATA[9]

MEM\_MB\_DATA10 MA\_DATA[10]

MEM\_MB\_DATA11 MA\_DATA[11]

MEM\_MB\_DATA12 MA\_DATA[12]

MEM\_MB\_DATA13 MA\_DATA[13]

MEM\_MB\_DATA14 MA\_DATA[14]

MEM\_MB\_DATA15 MA\_DATA[15]

MEM\_MB\_DATA16 MA\_DATA[16]

MEM\_MB\_DATA17 MA\_DATA[17]

MEM\_MB\_DATA18 MA\_DATA[18]

MEM\_MB\_DATA19 MA\_DATA[19]

MEM\_MB\_DATA20 MA\_DATA[20]

MEM\_MB\_DATA21 MA\_DATA[21]

MEM\_MB\_DATA22 MA\_DATA[22]

MEM\_MB\_DATA23 MA\_DATA[23]

MEM\_MB\_DATA24 MA\_DATA[24]

MEM\_MB\_DATA25 MA\_DATA[25]

MEM\_MB\_DATA26 MA\_DATA[26]

MEM\_MB\_DATA27 MA\_DATA[27]

MEM\_MB\_DATA28 MA\_DATA[28]

MEM\_MB\_DATA29 MA\_DATA[29]

MEM\_MB\_DATA30 MA\_DATA[30]

MEM\_MB\_DATA31 MA\_DATA[31]

MEM\_MB\_DATA32 MA\_DATA[32]

MEM\_MB\_DATA33 MA\_DATA[33]

MEM\_MB\_DATA34 MA\_DATA[34]

MEM\_MB\_DATA35 MA\_DATA[35]

MEM\_MB\_DATA36 MA\_DATA[36]

MEM\_MB\_DATA37 MA\_DATA[37]

MEM\_MB\_DATA38 MA\_DATA[38]

MEM\_MB\_DATA39 MA\_DATA[39]

MEM\_MB\_DATA40 MA\_DATA[40]

MEM\_MB\_DATA41 MA\_DATA[41]

MEM\_MB\_DATA42 MA\_DATA[42]

MEM\_MB\_DATA43 MA\_DATA[43]

MEM\_MB\_DATA44 MA\_DATA[44]

MEM\_MB\_DATA45 MA\_DATA[45]

MEM\_MB\_DATA46 MA\_DATA[46]

MEM\_MB\_DATA47 MA\_DATA[47]

MEM\_MB\_DATA48 MA\_DATA[48]

MEM\_MB\_DATA49 MA\_DATA[49]

MEM\_MB\_DATA50 MA\_DATA[50]

MEM\_MB\_DATA51 MA\_DATA[51]

MEM\_MB\_DATA52 MA\_DATA[52]

MEM\_MB\_DATA53 MA\_DATA[53]

MEM\_MB\_DATA54 MA\_DATA[54]

MEM\_MB\_DATA55 MA\_DATA[55]

MEM\_MB\_DATA56 MA\_DATA[56]

MEM\_MB\_DATA57 MA\_DATA[57]

MEM\_MB\_DATA58 MA\_DATA[58]

MEM\_MB\_DATA59 MA\_DATA[59]

MEM\_MB\_DATA60 MA\_DATA[60]

MEM\_MB\_DATA61 MA\_DATA[61]

MEM\_MB\_DATA62 MA\_DATA[62]

MEM\_MB\_DATA63 MA\_DATA[63]

MEM\_MB\_DM0 MA\_DM[0]

MEM\_MB\_DM1 MA\_DM[1]

MEM\_MB\_DM2 MA\_DM[2]

MEM\_MB\_DM3 MA\_DM[3]

MEM\_MB\_DM4 MA\_DM[4]

MEM\_MB\_DM5 MA\_DM[5]

MEM\_MB\_DM6 MA\_DM[6]

MEM\_MB\_DM7 MA\_DM[7]

MEM\_MB\_DQS0 MA\_DQS[0]

MEM\_MB\_DQS0#0 MA\_DQS[0]

MEM\_MB\_DQS1 MA\_DQS[1]

MEM\_MB\_DQS1#1 MA\_DQS[1]

MEM\_MB\_DQS2 MA\_DQS[2]

MEM\_MB\_DQS2#2 MA\_DQS[2]

MEM\_MB\_DQS3 MA\_DQS[3]

MEM\_MB\_DQS3#3 MA\_DQS[3]

MEM\_MB\_DQS4 MA\_DQS[4]

MEM\_MB\_DQS4#4 MA\_DQS[4]

MEM\_MB\_DQS5 MA\_DQS[5]

MEM\_MB\_DQS5#5 MA\_DQS[5]

MEM\_MB\_DQS6 MA\_DQS[6]

MEM\_MB\_DQS6#6 MA\_DQS[6]

MEM\_MB\_DQS7 MA\_DQS[7]

MEM\_MB\_DQS7#7 MA\_DQS[7]

MEM\_MB\_DATA0 E12

MEM\_MB\_DATA1 E12

MEM\_MB\_DATA2 H14

MEM\_MB\_DATA3 G14

MEM\_MB\_DATA4 H11

MEM\_MB\_DATA5 H12

MEM\_MB\_DATA6 C13

MEM\_MB\_DATA7 H13

MEM\_MB\_DATA8 H15

MEM\_MB\_DATA9 E15

MEM\_MB\_DATA10 E17

MEM\_MB\_DATA11 H17

MEM\_MB\_DATA12 E14

MEM\_MB\_DATA13 F14

MEM\_MB\_DATA14 C17

MEM\_MB\_DATA15 G17

MEM\_MB\_DATA16 G18

MEM\_MB\_DATA17 C19

MEM\_MB\_DATA18 D22

MEM\_MB\_DATA19 E20

MEM\_MB\_DATA20 E18

MEM\_MB\_DATA21 F18

MEM\_MB\_DATA22 B22

MEM\_MB\_DATA23 C23

MEM\_MB\_DATA24 F20

MEM\_MB\_DATA25 F22

MEM\_MB\_DATA26 H24

MEM\_MB\_DATA27 H19

MEM\_MB\_DATA28 E21

MEM\_MB\_DATA29 E22

MEM\_MB\_DATA30 H20

MEM\_MB\_DATA31 H22

MEM\_MB\_DATA32 Y24

MEM\_MB\_DATA33 AB24

MEM\_MB\_DATA34 AB22

MEM\_MB\_DATA35 AA21

MEM\_MB\_DATA36 W22

MEM\_MB\_DATA37 W21

MEM\_MB\_DATA38 Y22

MEM\_MB\_DATA39 AA22

MEM\_MB\_DATA40 Y20

MEM\_MB\_DATA41 AA20

MEM\_MB\_DATA42 AA18

MEM\_MB\_DATA43 AB18

MEM\_MB\_DATA44 AB21

MEM\_MB\_DATA45 AD21

MEM\_MB\_DATA46 AD19

MEM\_MB\_DATA47 Y19

MEM\_MB\_DATA48 AD17

MEM\_MB\_DATA49 W16

MEM\_MB\_DATA50 W14

MEM\_MB\_DATA51 Y14

MEM\_MB\_DATA52 Y17

MEM\_MB\_DATA53 AB17

MEM\_MB\_DATA54 AB15

MEM\_MB\_DATA55 AD15

MEM\_MB\_DATA56 AB13

MEM\_MB\_DATA57 AD13

MEM\_MB\_DATA58 Y12

MEM\_MB\_DATA59 W11

MEM\_MB\_DATA60 AB14

MEM\_MB\_DATA61 AB14

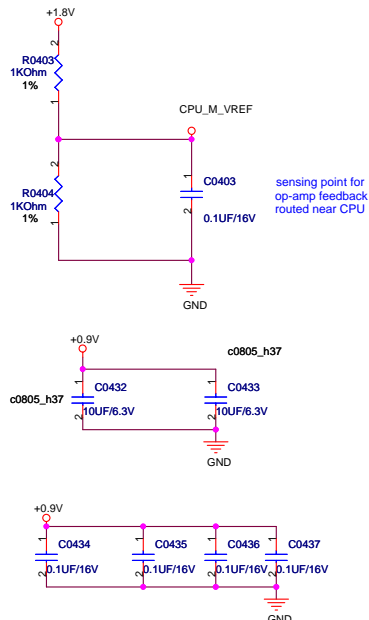
MEM\_MB\_DATA62 AB12

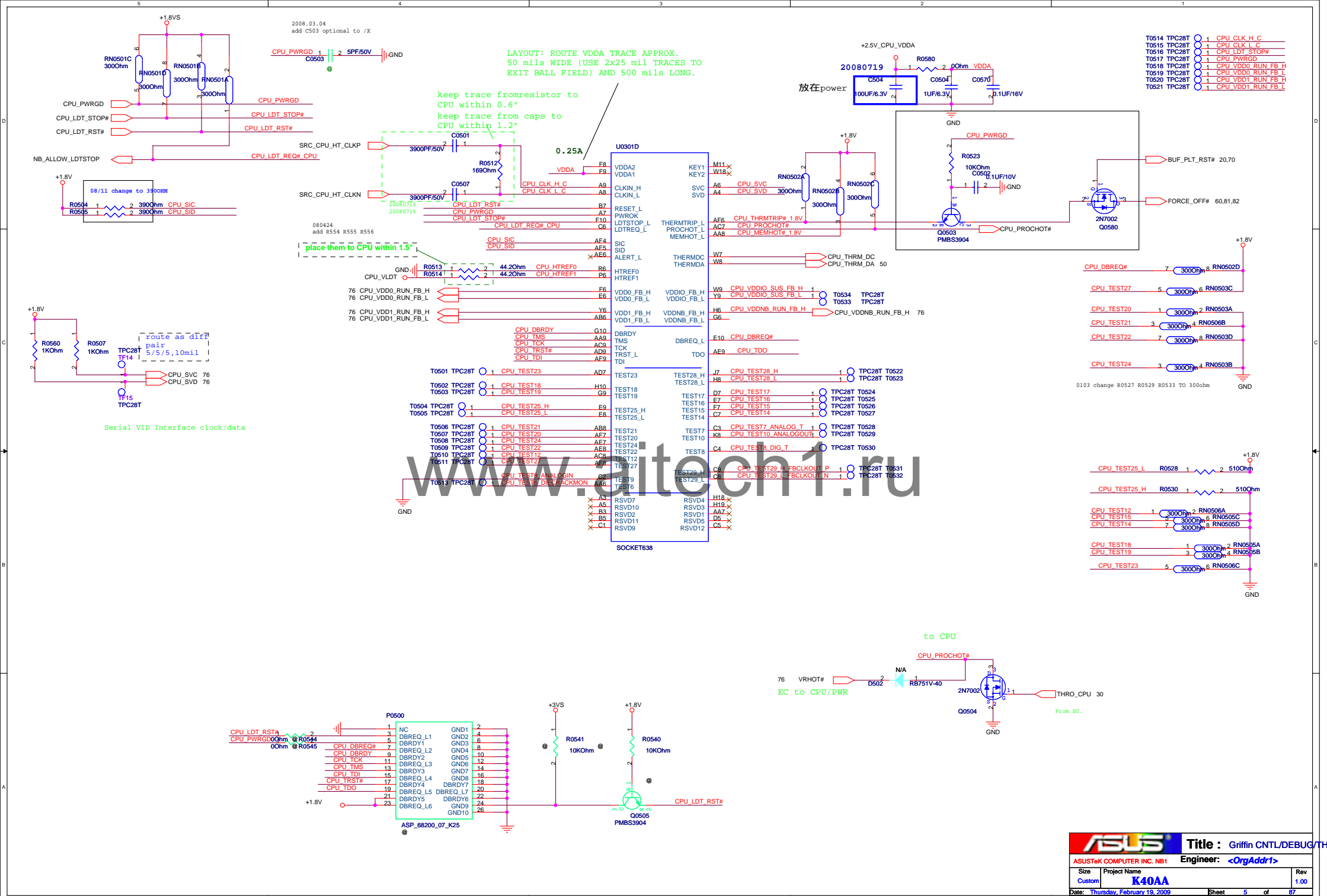
MEM\_MB\_DATA63 AB12

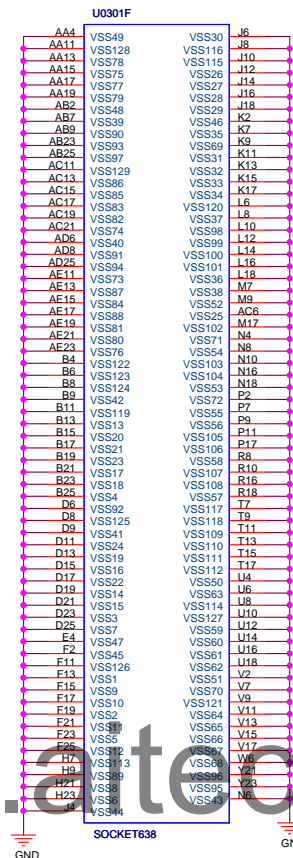
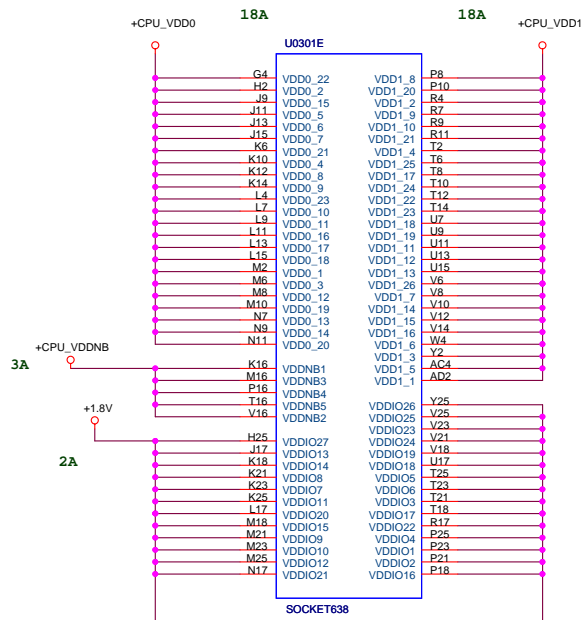
MEM\_MB\_DM0 E12

MEM\_MB\_DM1

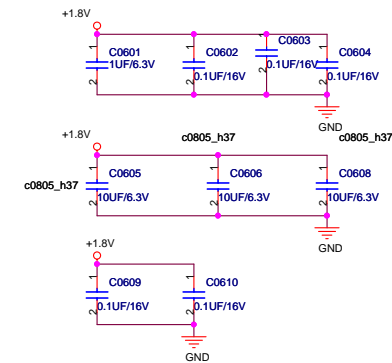
09/23 2.0



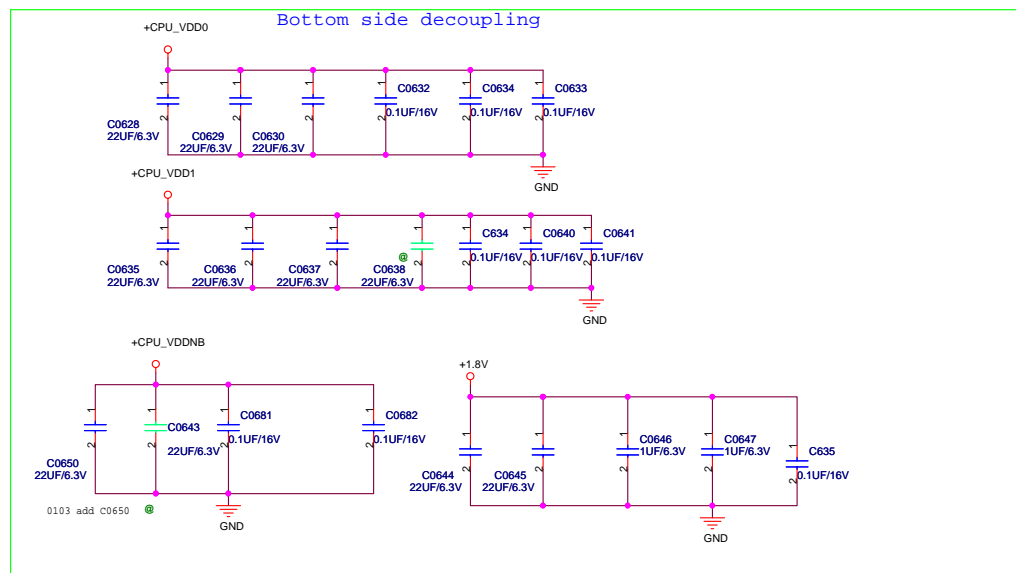




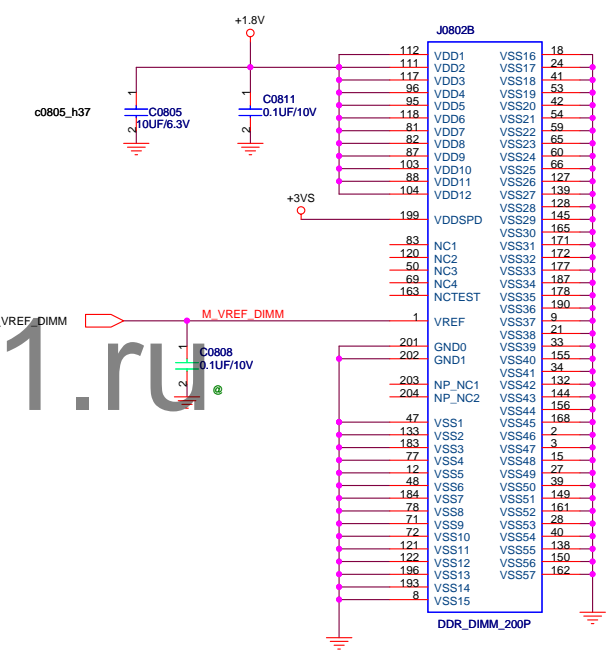
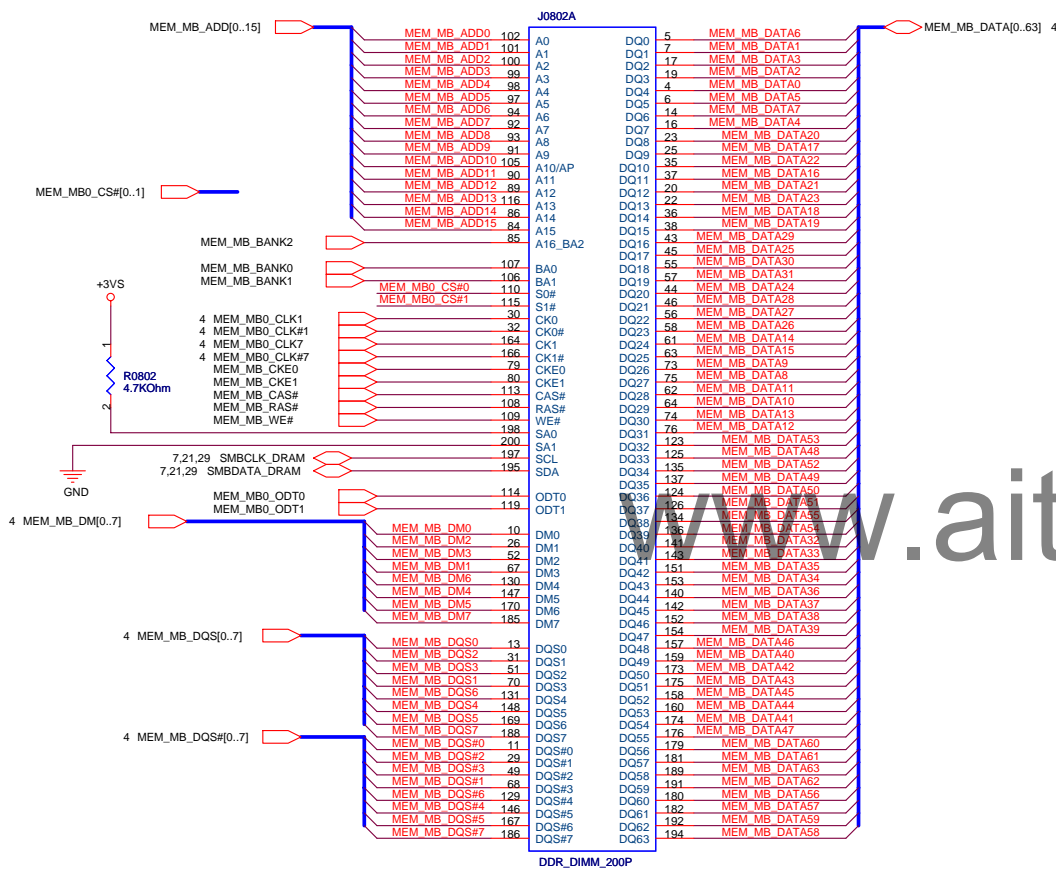
Decoupling between Processor and DIMMs, Place close to Porcessor as possible



www.aitech1.ru place close to socket

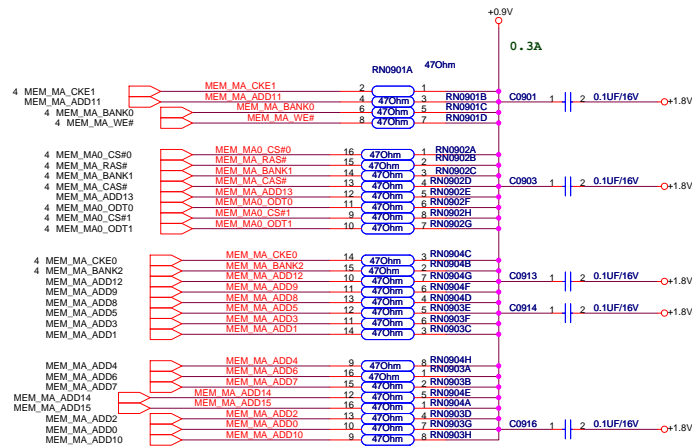




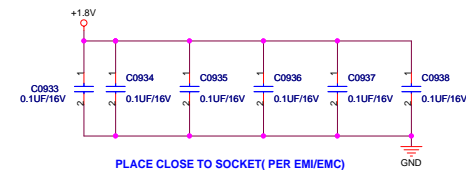
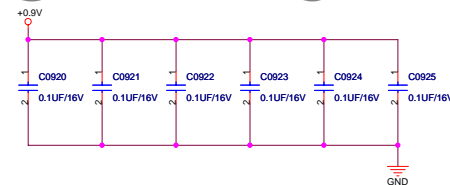
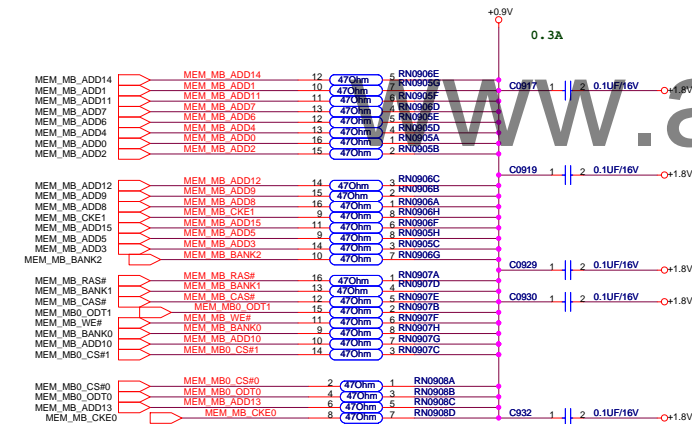
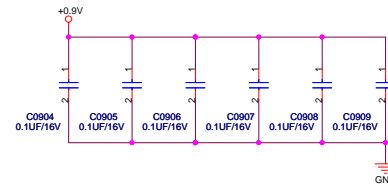


low

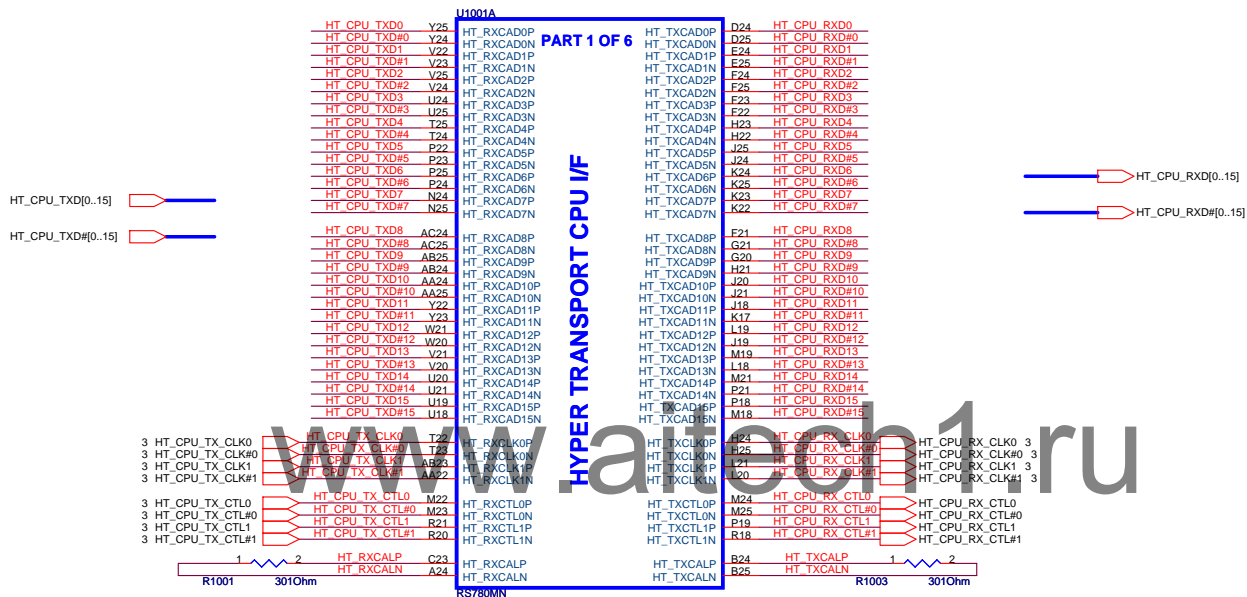




20080803 Remove R907



PLACE CLOSE TO SOCKET( PER EMI/EMC)



70 GFX\_VGA\_RXP[0..15]  
70 GFX\_VGA\_RXN[0..15]

PCI-E:  
0-3 HDMI@ RS780M  
4-7 NC  
8-15 VGA8x

U1001B  
GFX\_VGA\_RXP0 D4  
GFX\_VGA\_RXN0 C4  
GFX\_VGA\_RXP1 A3  
GFX\_VGA\_RXN1 B3  
GFX\_VGA\_RXP2 C2  
GFX\_VGA\_RXN2 C1  
GFX\_VGA\_RXP3 E5  
GFX\_VGA\_RXN3 F5  
GFX\_VGA\_RXP4 G6  
GFX\_VGA\_RXN4 H6  
GFX\_VGA\_RXP5 H5  
GFX\_VGA\_RXN5 H6  
GFX\_VGA\_RXP6 J6  
GFX\_VGA\_RXN6 J5  
GFX\_VGA\_RXP7 J7  
GFX\_VGA\_RXN7 L5  
GFX\_VGA\_RXP8 L6  
GFX\_VGA\_RXN8 L5  
GFX\_VGA\_RXP9 M8  
GFX\_VGA\_RXN9 L8  
GFX\_VGA\_RXP10 P7  
GFX\_VGA\_RXN10 M7  
GFX\_VGA\_RXP11 P5  
GFX\_VGA\_RXN11 M5  
GFX\_VGA\_RXP12 P8  
GFX\_VGA\_RXN12 R8  
GFX\_VGA\_RXP13 R6  
GFX\_VGA\_RXN13 R5  
GFX\_VGA\_RXP14 P4  
GFX\_VGA\_RXN14 P3  
GFX\_VGA\_RXP15 T4  
GFX\_VGA\_RXN15 T3

PART 2 OF 6

PCI-E I/F GFX

GFX\_TX0P A5  
GFX\_TX0N B5  
GFX\_TX1P A4  
GFX\_TX1N B4  
GFX\_TX2P C3  
GFX\_TX2N B2  
GFX\_TX3P D1  
GFX\_TX3N E1  
GFX\_TX4P F4  
GFX\_TX4N F3  
GFX\_TX5P F2  
GFX\_TX5N F1  
GFX\_TX6P H4  
GFX\_TX6N H3  
GFX\_TX7P H1  
GFX\_TX7N H2  
GFX\_TX8P J1  
GFX\_TX8N J2  
GFX\_TX9P J4  
GFX\_TX9N K4  
GFX\_TX10P K1  
GFX\_TX10N K2  
GFX\_TX11P M4  
GFX\_TX11N M3  
GFX\_TX12P M1  
GFX\_TX12N M2  
GFX\_TX13P N1  
GFX\_TX13N N2  
GFX\_TX14P P1  
GFX\_TX14N P2  
GFX\_TX15P P2  
GFX\_TX15N P2

GPP\_TX0P AC1  
GPP\_TX0N AC2  
GPP\_TX1P AB3  
GPP\_TX1N AB4  
GPP\_TX2P AB3  
GPP\_TX2N AB4  
GPP\_TX3P Y1  
GPP\_TX3N Y2  
GPP\_TX4P Y4  
GPP\_TX4N Y3  
GPP\_TX5P V1  
GPP\_TX5N V2

PCI\_E\_RXP1\_LAN  
PCI\_E\_RXN1\_LAN  
53 PCI\_E\_RXP2\_WLAN  
53 PCI\_E\_RXN2\_WLAN

PCI-E I/F GPP

SB\_RX0P AA8  
SB\_RX0N Y8  
SB\_RX1P AA7  
SB\_RX1N Y7  
SB\_RX2P AA6  
SB\_RX2N W5  
SB\_RX3P W5  
SB\_RX3N Y5

PCI-E I/F SB

SB\_TX0P AD7  
SB\_TX0N AE7  
SB\_TX1P AD6  
SB\_TX1N AE6  
SB\_TX2P AD6  
SB\_TX2N AE6  
SB\_TX3P AD5  
SB\_TX3N AE5

PCE\_CALRP  
PCE\_CALRN

RS780MN

1.27KOHM  
2KOHM

R1101  
R1102

+1.1V\_NB  
GND

PCIENB_TXN15	C1170	1	0.1UF/10V	GFX_VGA_TXN15
PCIENB_TXN14	C1167	1	0.1UF/10V	GFX_VGA_TXN14
PCIENB_TXN13	C1171	1	0.1UF/10V	GFX_VGA_TXN13
PCIENB_TXN12	C1169	1	0.1UF/10V	GFX_VGA_TXN12
PCIENB_TXN11	C1168	1	0.1UF/10V	GFX_VGA_TXN11
PCIENB_TXN10	C1172	1	0.1UF/10V	GFX_VGA_TXN10
PCIENB_TXN9	C1166	1	0.1UF/10V	GFX_VGA_TXN9
PCIENB_TXN8	C1165	1	0.1UF/10V	GFX_VGA_TXN8
PCIENB_TXN0	C1142	1	0.1UF/10V	GFX_VGA_TXN0
PCIENB_TXN1	C1144	1	0.1UF/10V	GFX_VGA_TXN1
PCIENB_TXN2	C1141	1	0.1UF/10V	GFX_VGA_TXN2
PCIENB_TXN3	C1148	1	0.1UF/10V	GFX_VGA_TXN3
PCIENB_TXN4	C1145	1	0.1UF/10V	GFX_VGA_TXN4
PCIENB_TXN5	C1147	1	0.1UF/10V	GFX_VGA_TXN5
PCIENB_TXN6	C1143	1	0.1UF/10V	GFX_VGA_TXN6
PCIENB_TXN7	C1146	1	0.1UF/10V	GFX_VGA_TXN7

70 GFX\_VGA\_TXN[0..15]

PCIENB_TXP15	C1163	1	0.1UF/10V	GFX_VGA_TXP15
PCIENB_TXP14	C1161	1	0.1UF/10V	GFX_VGA_TXP14
PCIENB_TXP13	C1160	1	0.1UF/10V	GFX_VGA_TXP13
PCIENB_TXP12	C1164	1	0.1UF/10V	GFX_VGA_TXP12
PCIENB_TXP11	C1162	1	0.1UF/10V	GFX_VGA_TXP11
PCIENB_TXP10	C1158	1	0.1UF/10V	GFX_VGA_TXP10
PCIENB_TXP9	C1157	1	0.1UF/10V	GFX_VGA_TXP9
PCIENB_TXP8	C1159	1	0.1UF/10V	GFX_VGA_TXP8
PCIENB_TXP0	C1149	1	0.1UF/10V	GFX_VGA_TXP0
PCIENB_TXP1	C1150	1	0.1UF/10V	GFX_VGA_TXP1
PCIENB_TXP2	C1151	1	0.1UF/10V	GFX_VGA_TXP2
PCIENB_TXP3	C1156	1	0.1UF/10V	GFX_VGA_TXP3
PCIENB_TXP4	C1152	1	0.1UF/10V	GFX_VGA_TXP4
PCIENB_TXP5	C1155	1	0.1UF/10V	GFX_VGA_TXP5
PCIENB_TXP6	C1153	1	0.1UF/10V	GFX_VGA_TXP6
PCIENB_TXP7	C1154	1	0.1UF/10V	GFX_VGA_TXP7

70 GFX\_VGA\_TXP[0..15]

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NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

2008.03.03 add R1203 R1204 R1205 R1203 14009R for RS780 A13	150R termination < 1 inch trace
73 CRT_RED_GM	1500hm 2 1% R1203
73 CRT_GREEN_GM	1500hm 2 1% R1204
73 CRT_BLUE_GM	1500hm 2 1% R1205

RS780 POWERGOOD  
is 1.8VS rail

OSC_14M_NB 1.1V 158R/90.9R
-------------------------------

20080716 HDMI Power DDC???

PU@ conn side.

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

0104 ADD

CPU\_LDT\_STOP# NB\_LDT\_STOP#

NB\_ALLOW\_LDTSTOP NB\_ALLOW\_LDTSTOP\_NB

20080716 Remove the STRP\_DATA Solution

PART 3 OF 6

CRT/VOUT

FM PLL PWR

CLOCKS

MIS.

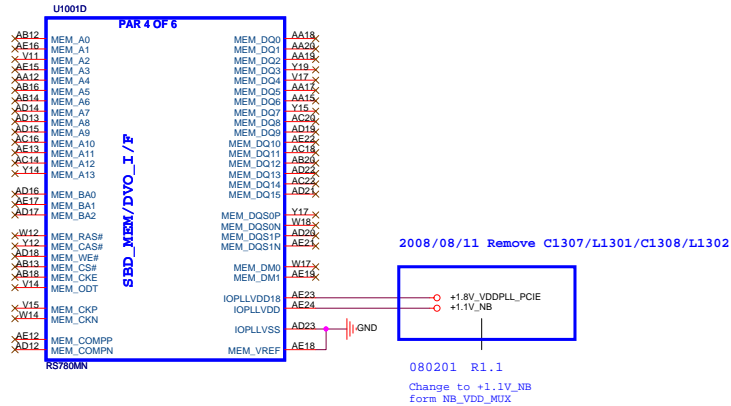
LVTM

2008.08.04  
the U and L of LVDS exchange

change backlight enable  
pin from LVDS\_ENA\_BL to  
LVDS\_BLOW

?? for external graphic

R1.11 080319  
Change the NB Part number to RS780 (A13)



#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS780:SUS\_STAT

#### STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

Enables the Test Debug Bus using PCIE bus:

1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

RS780: configurable thru register setting only

#### RS740/RS780: Enables Side port memory

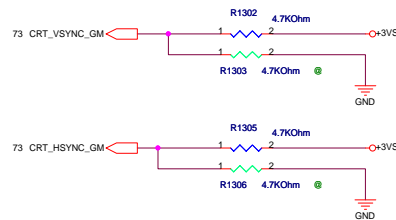
RS780:HSYNCH

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available  
0 = Memory Side port available


Register Readback of strap: NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]


080118  
Disable Side Port Memory  
R1.1






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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
A	K40AA		1.00
Date: Monday, February 09, 2009		Sheet	15 of 87

		<b>Title :</b> BLANK	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	K40AA	1.00	
Date: Monday, February 09, 2009		Sheet	16 of 87




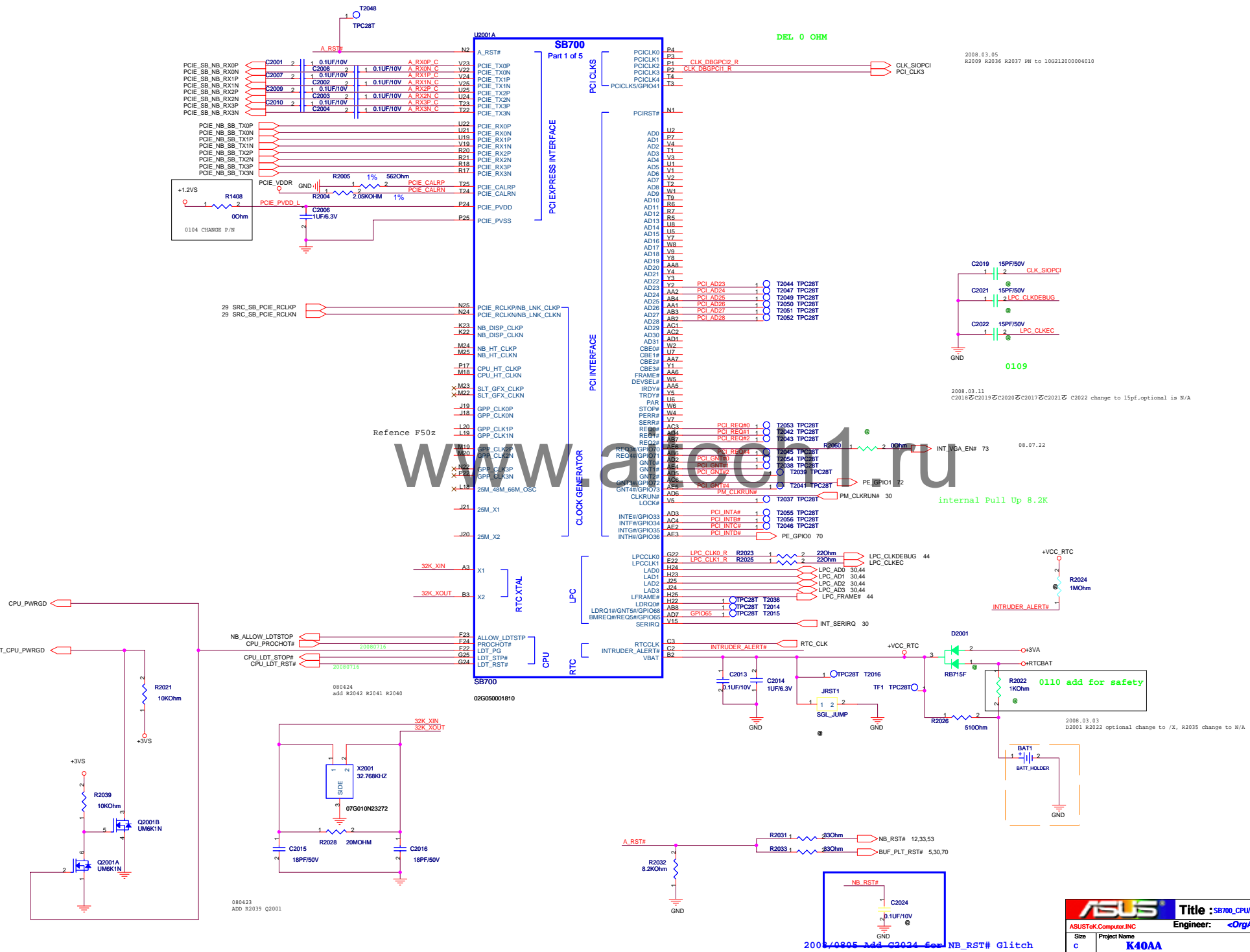
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
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			Title : BLANK		
ASUSTeK COMPUTER INC			Engineer:		
Size	Project Name				Rev
A	K40AA				1.00
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ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
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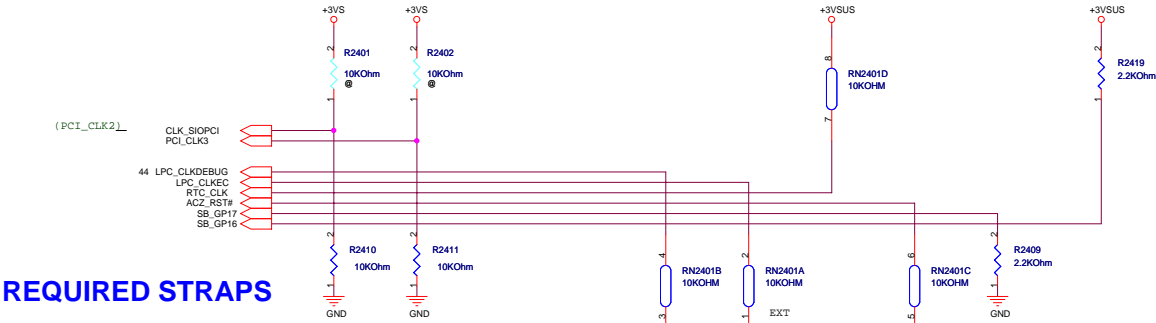








NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK




	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	32-kHz clock ENABLED	INTERNAL RTC DEFAULT	Integrated Microcontroller ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	32-kHz clock DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	Integrated Microcontroller DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWB ROM	


WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.  
I.E. LPC\_CLK0 FOR EC ENABLE, AZ\_RST# FOR MEM BOOT ENABLE.




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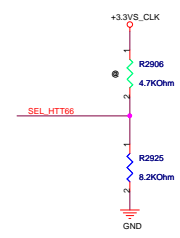
			Title : BLANK		
ASUSTeK COMPUTER INC			Engineer:		
Size	Project Name			Rev	
A	K40AA			1.00	
Date: Monday, February 09, 2009		Sheet 26		of	87

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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
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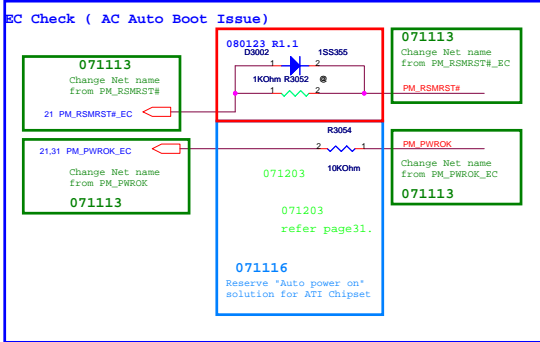
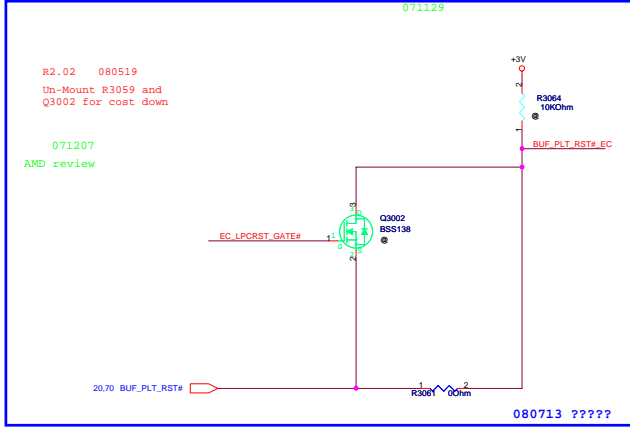
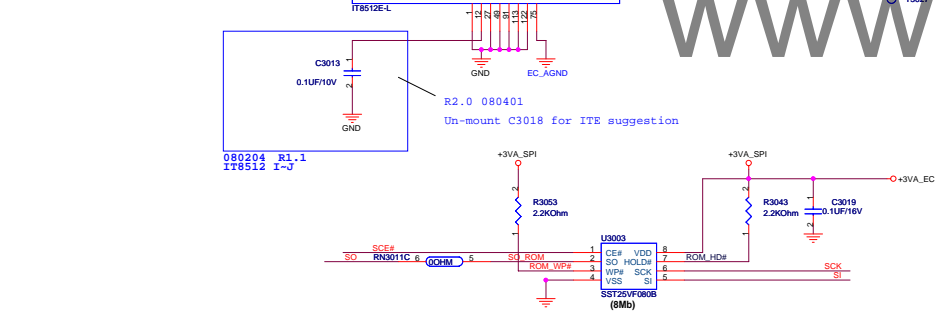


SEL_27	0	100 MHz differential Spread SRC clock
	1	27MHz 3.3V 27MHz spread clock

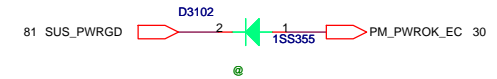
SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

Change RNX3001 from 47 ohm to 0 ohm .The RNX3001 with modification of RN4401 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.



**Note:** When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

R1.1



080123 Reserve for SB700 interface

12G09103004P

**Touchpad Connector**

For Side SW

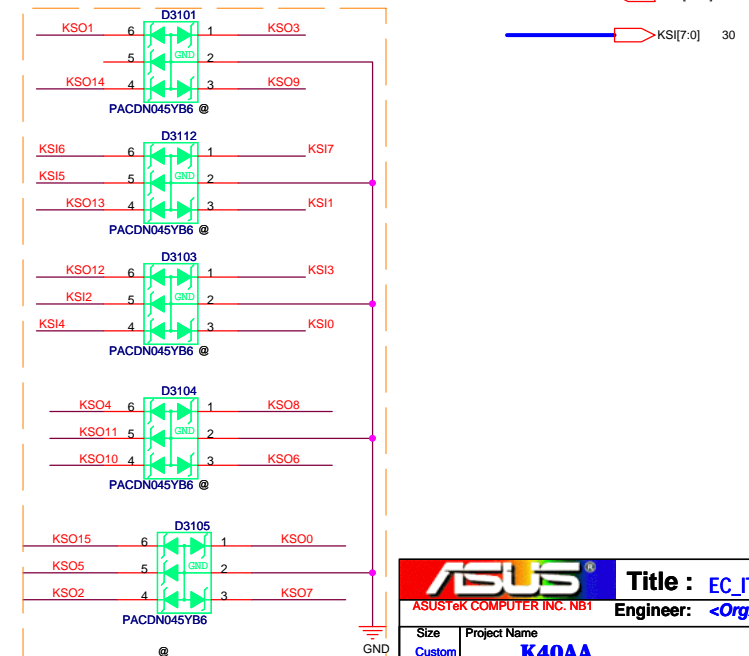
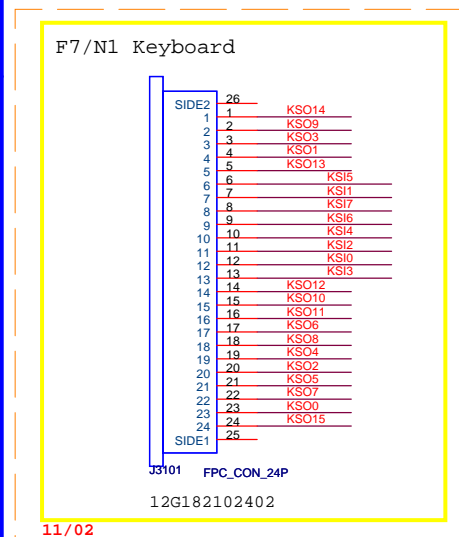
check

R1.1 081031-2

PWR  
SWITCH

Note:  
LID\_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

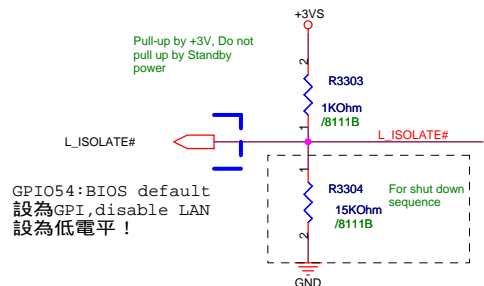
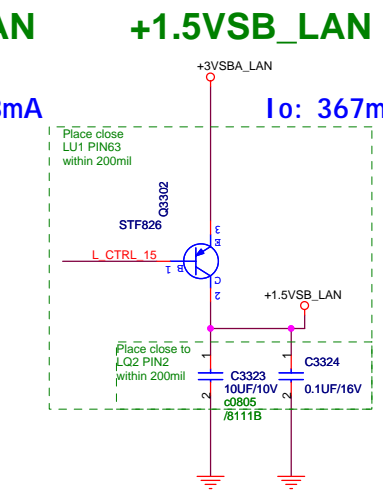
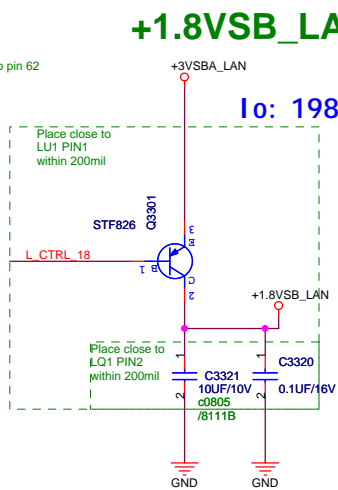
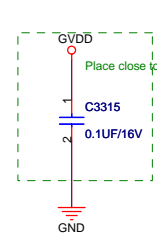
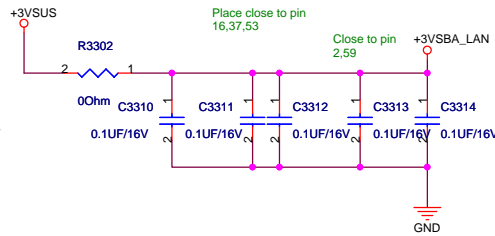
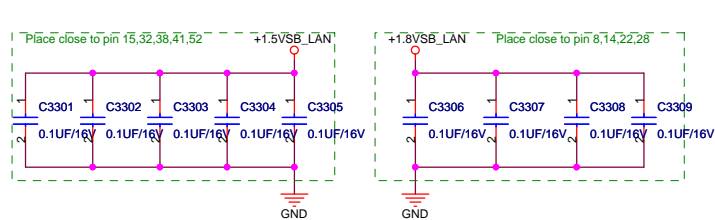
del CN3201.....CN3206



D3106,R3105,R3106,Q3101, and Q3102, for cost down

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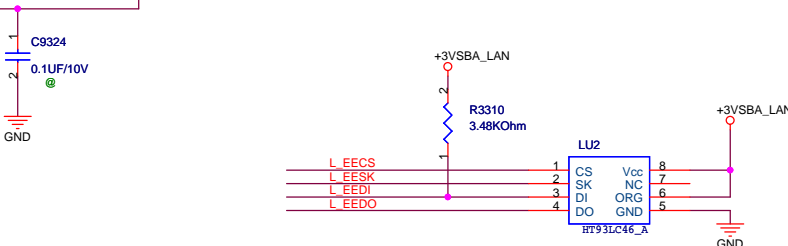
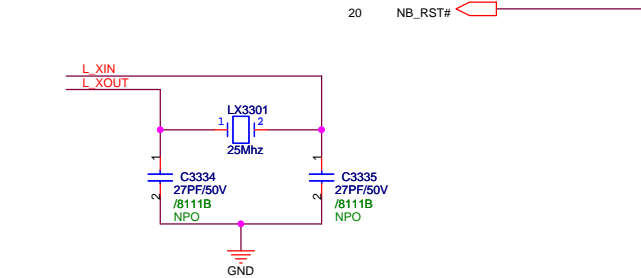
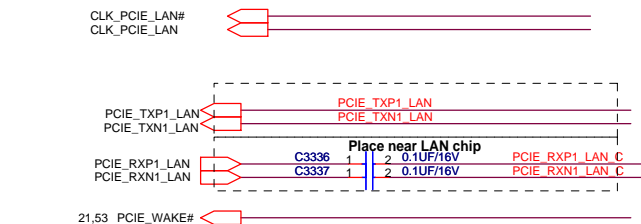
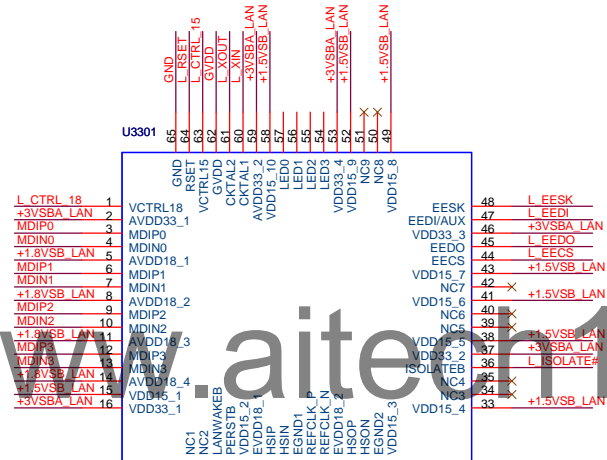


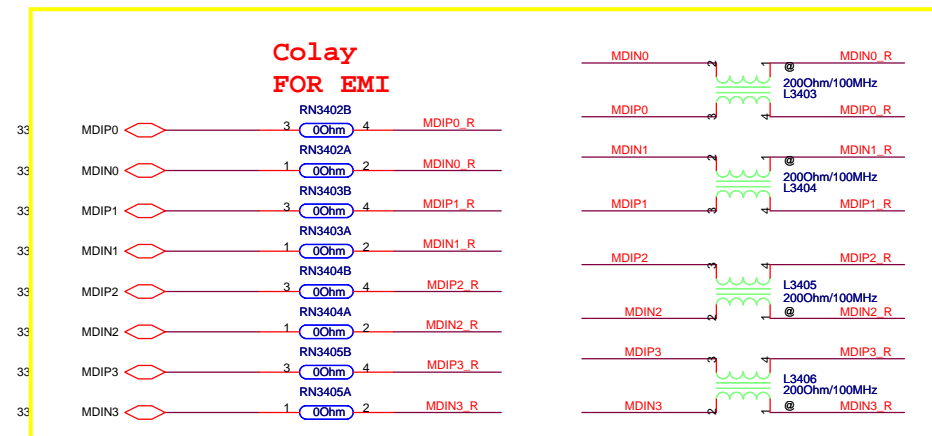
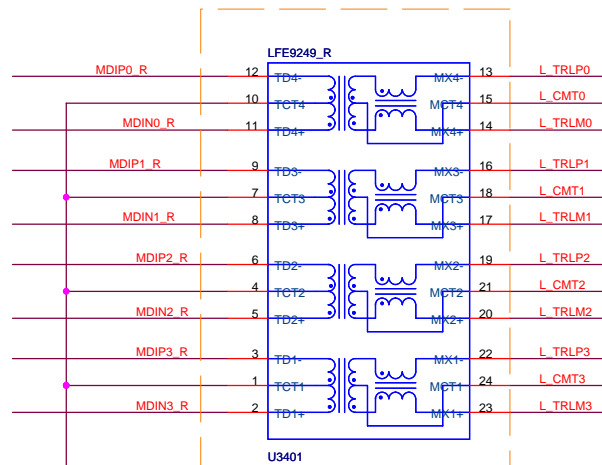


GPIO54:BIOS default  
設為GPI,disable LAN  
設為低電平!

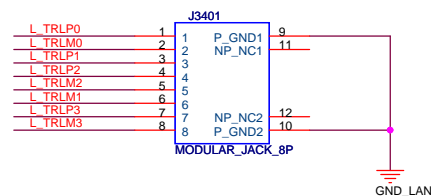
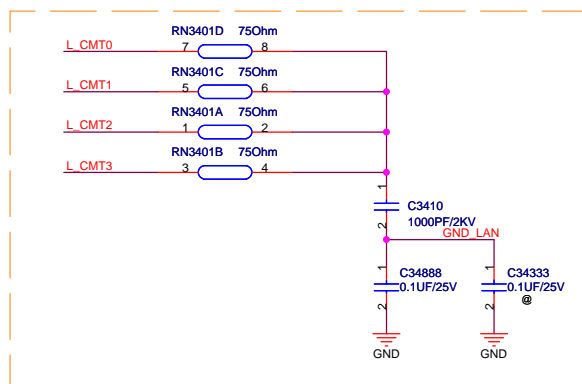


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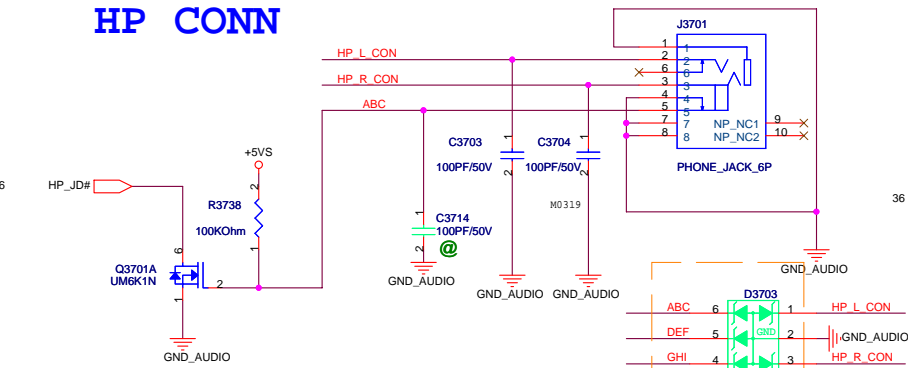
www.aitech1.ru



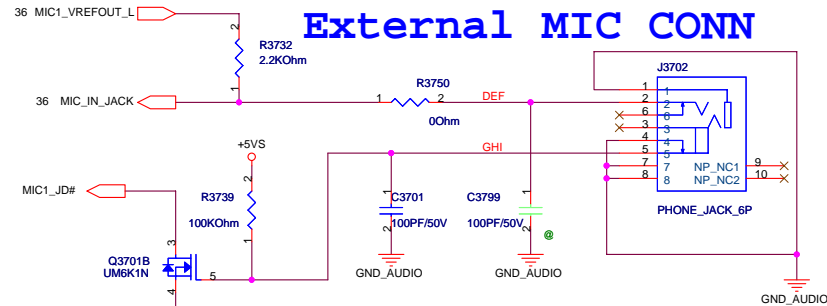
www.aitech1.ru



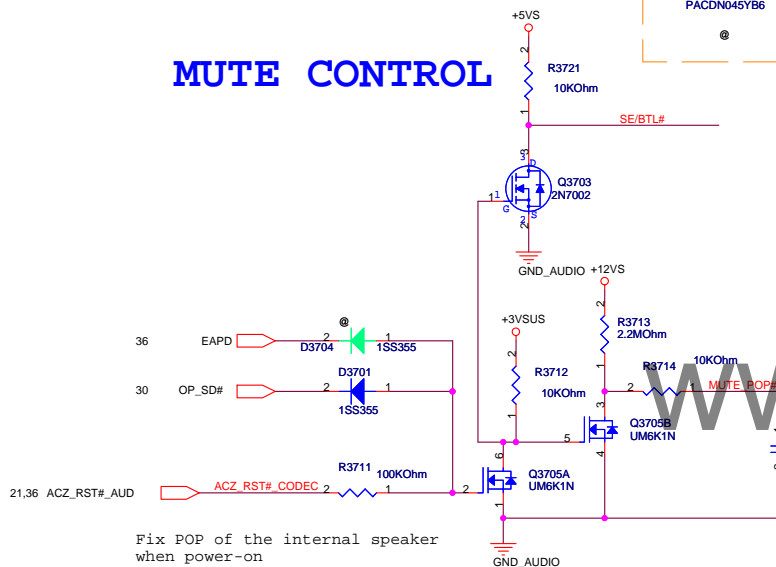
## HP CONN



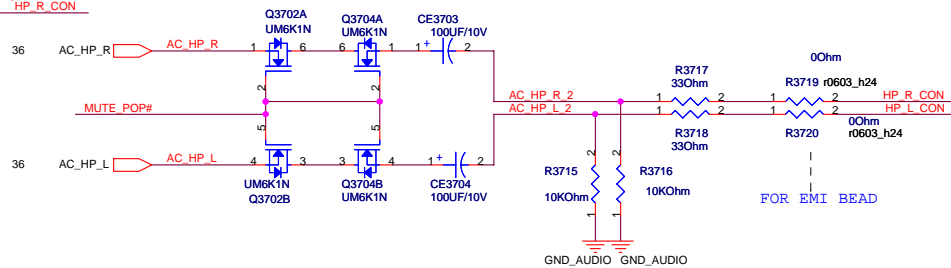
## External MIC CONN



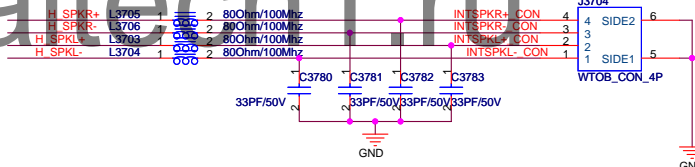
## MUTE CONTROL



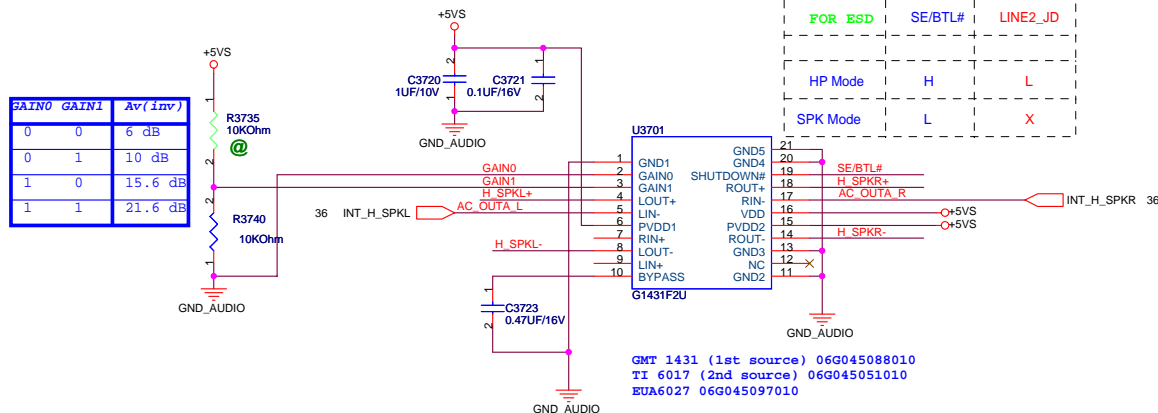
Fix POP of the internal speaker when power-on



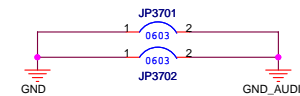
## SPEAKER CONNECTOR (2W)



## SPEAKER AMP




GMT 1431 (1st source) 06G045088010  
TI 6017 (2nd source) 06G045051010  
EUA6027 06G045097010



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Size A	Project Name K40AA		Rev 1.00
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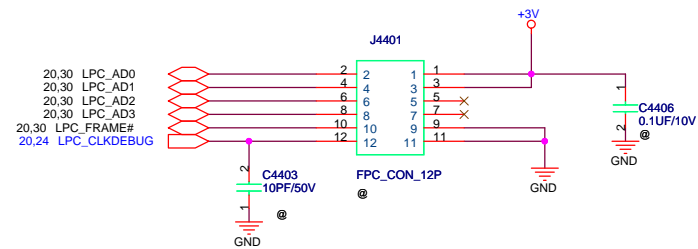
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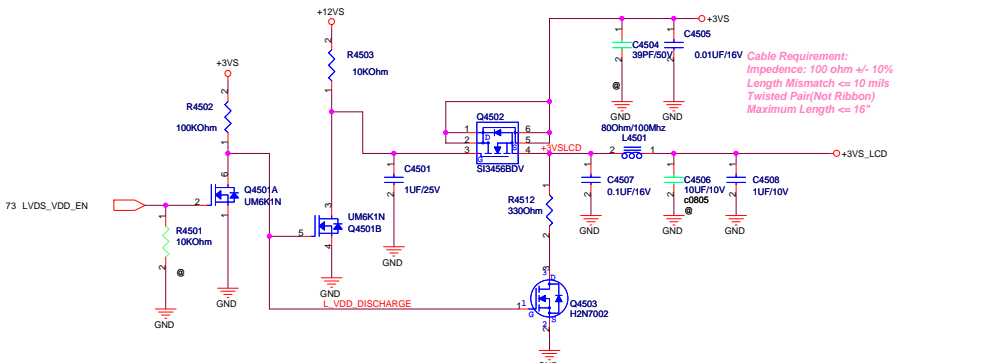
If don't support NewCard Debug Card,Pls do  
(a) DNI all components of block A  
(b) Mount Block C (RN5401,R6975)

### For PCMCIA Debug Card

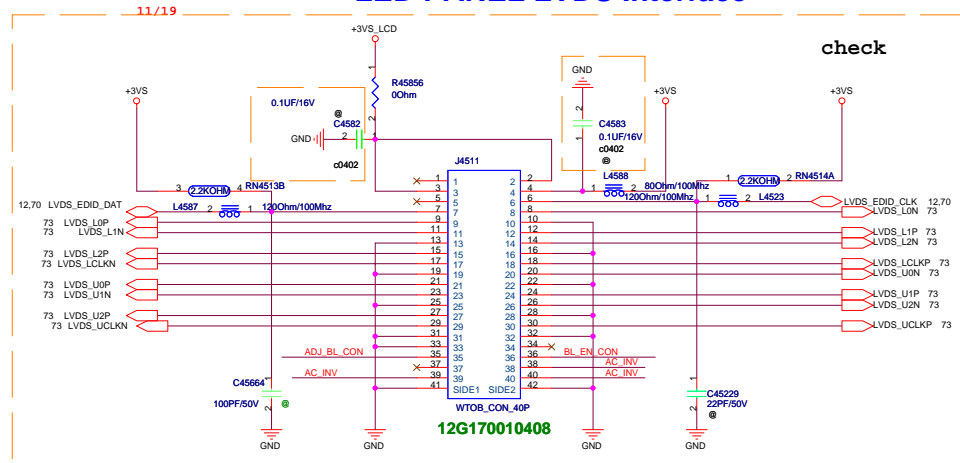
If support NewCard Debug Card,  
Pls don't mount all components.

## LCD Backlight Control

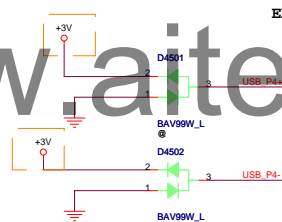
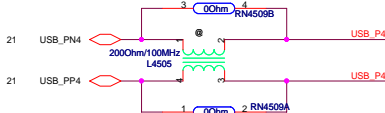
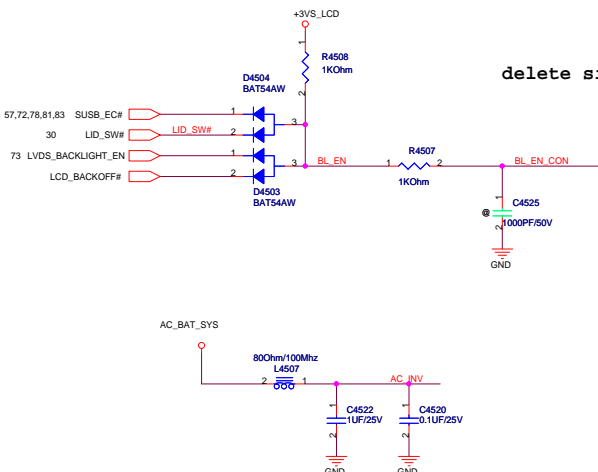
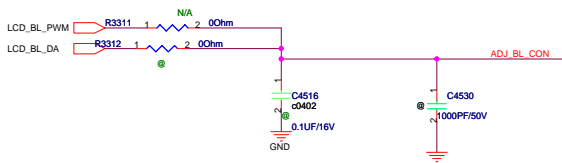
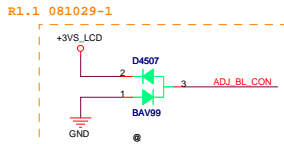
## LCD Power



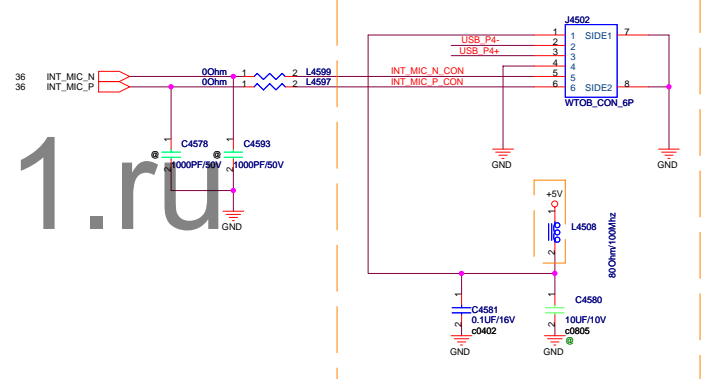
## LED PANEL LVDS Interface



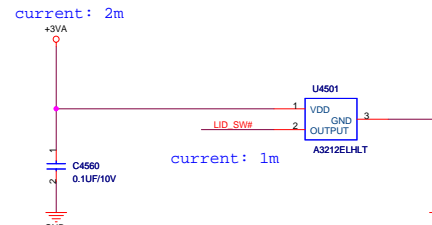
**INVERTER**  
**Interface/Speaker CONN.**



## CAMERA & MIC




## Hall effect switch






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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Monday, February 09, 2009		Sheet 47 of 87	

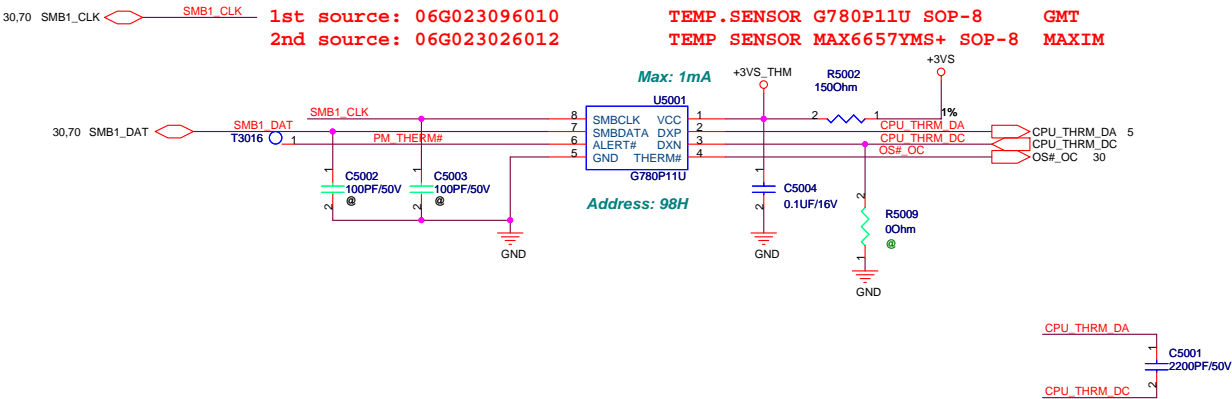
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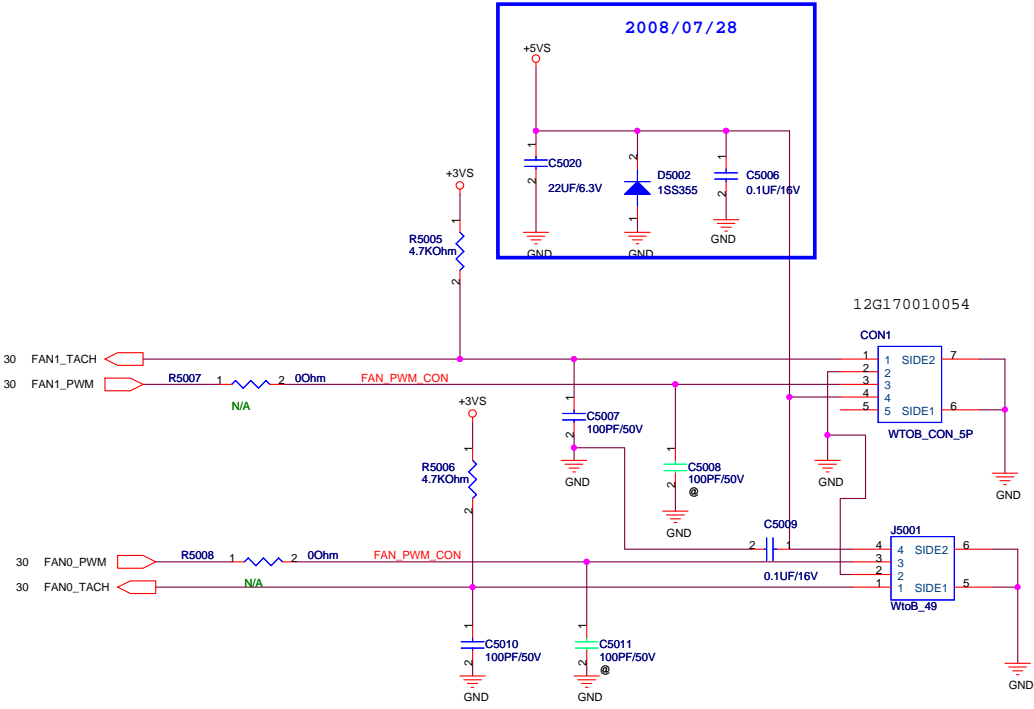
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
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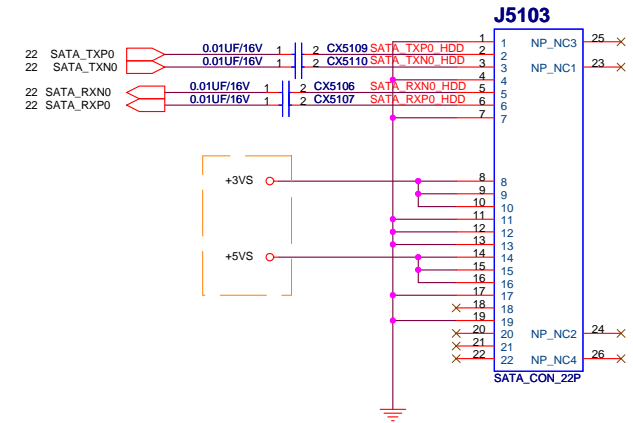
Thermal Sensor



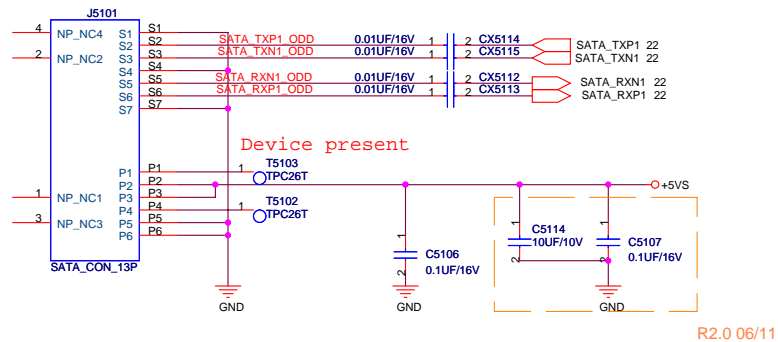
DC FAN Control



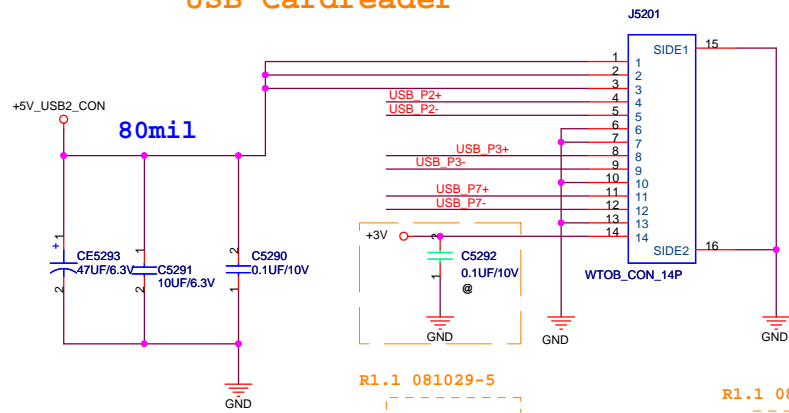
***ODD***



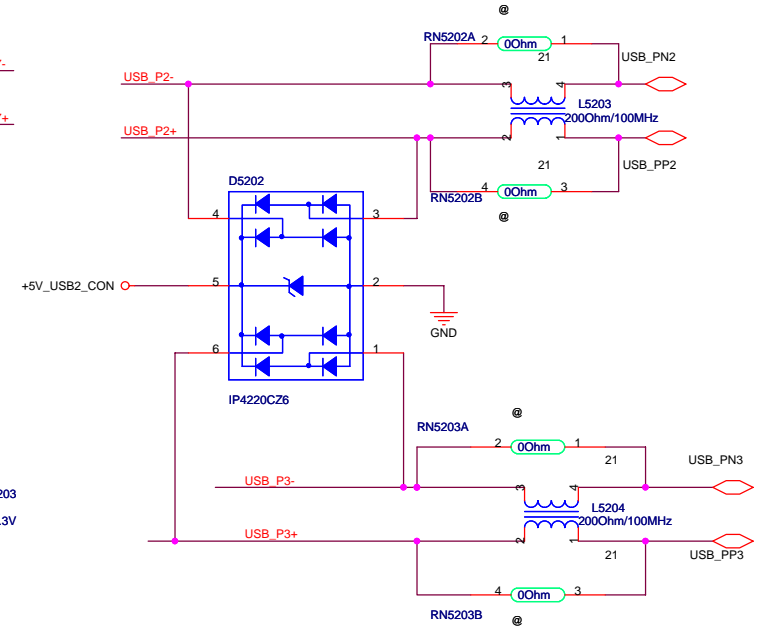
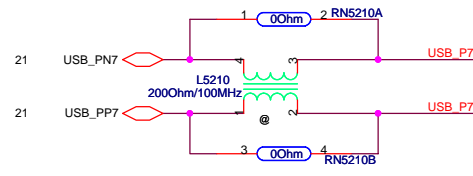
[www.aitech1.ru](http://www.aitech1.ru)



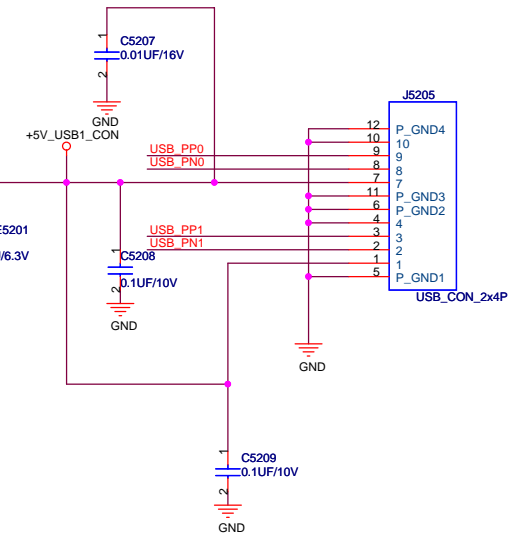
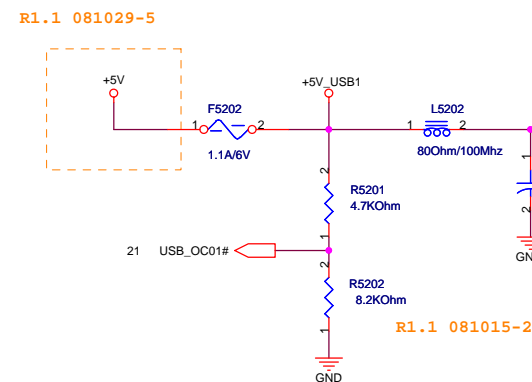
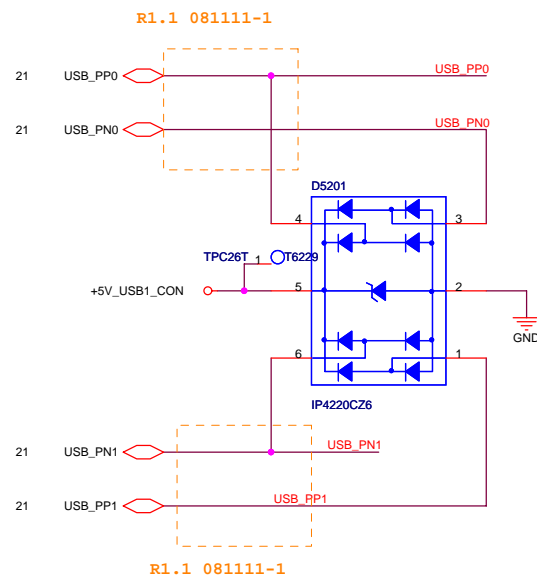
## USB Cardreader

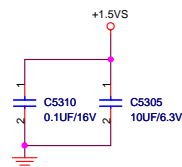


## USB Cardreader




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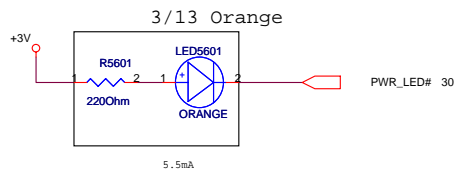
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ASUSTeK COMPUTER INC		Engineer:	
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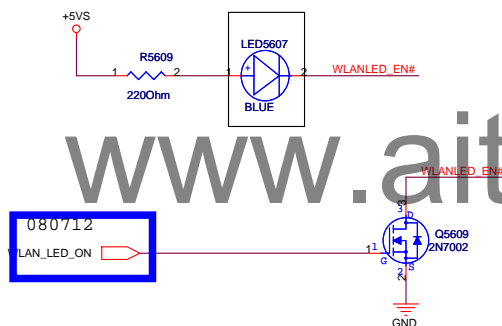
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
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### For Power LED



### For Ionizer

### For WireLess LED

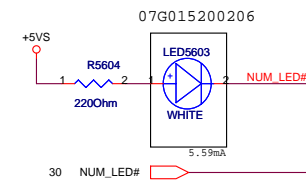


2008/07/30 Remove 3G Function

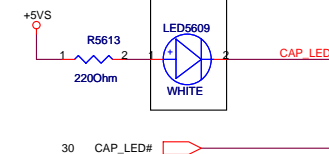
### LEDs for testing

2008/07/29 Remove 3G LED

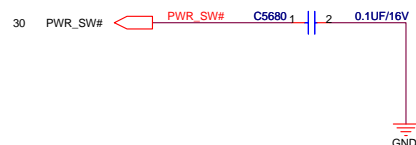
### For Number Lock



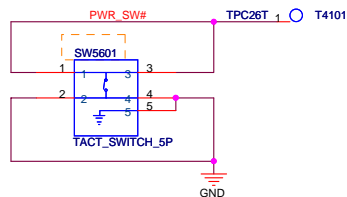
### For Caps. Lock



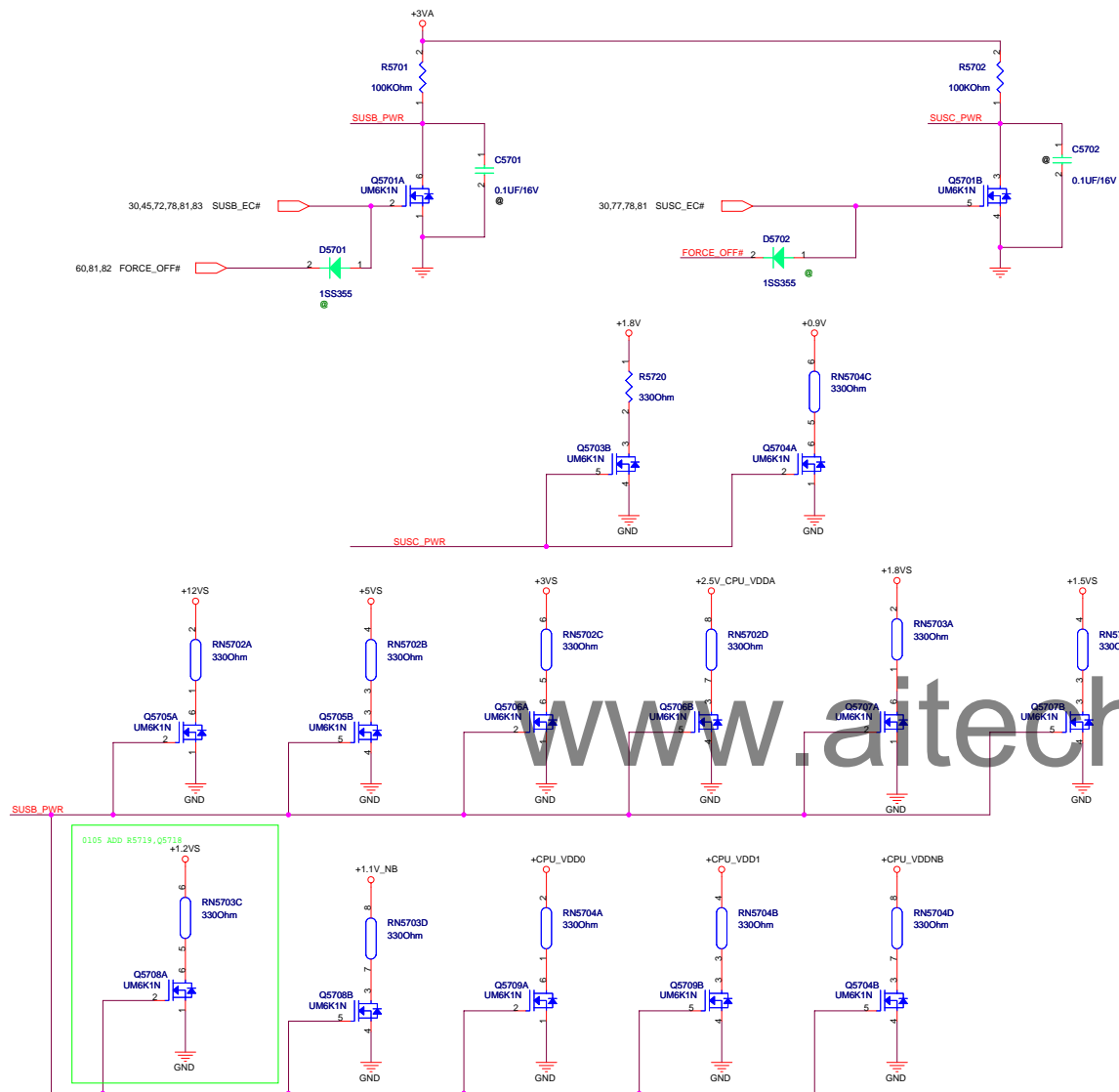
SW



SHUT\_DOWN#






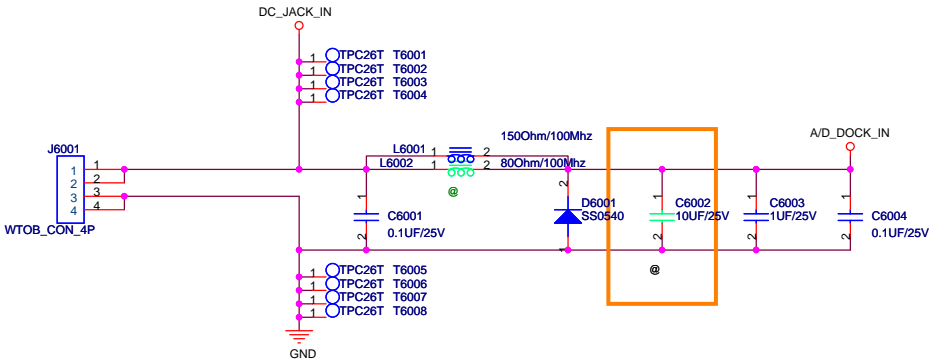


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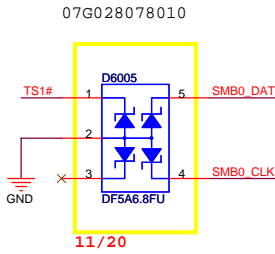
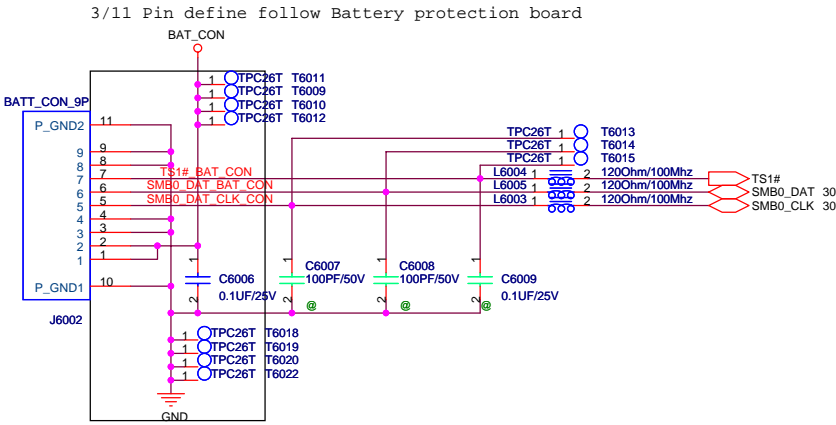
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name K40AA		Rev 1.00
Date: Monday, February 09, 2009		Sheet	59 of 87

DC IN

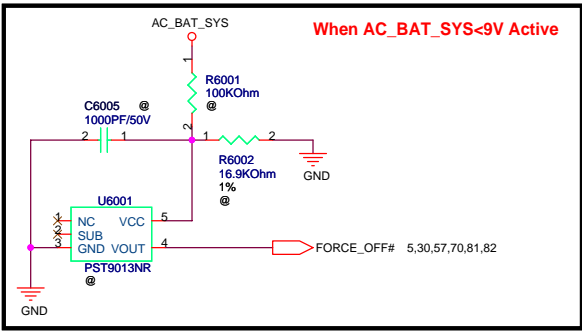


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BAT IN



Without Battery & Pull out Adapter



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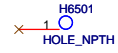
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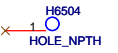
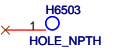
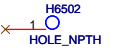
		Title : BLANK	
ASUSTeK COMPUTER INC.		Engineer:	
Drawn by	Project Name	Rev	Rev
D	K40AA	1	1.00
Date: 2008.11.20 14:00:00		Drawn by	Rev



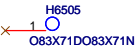
# Hole-A



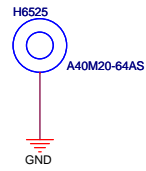
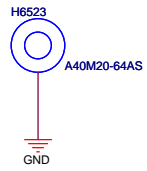
# Hole-B



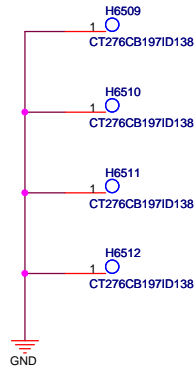
# Hole-C



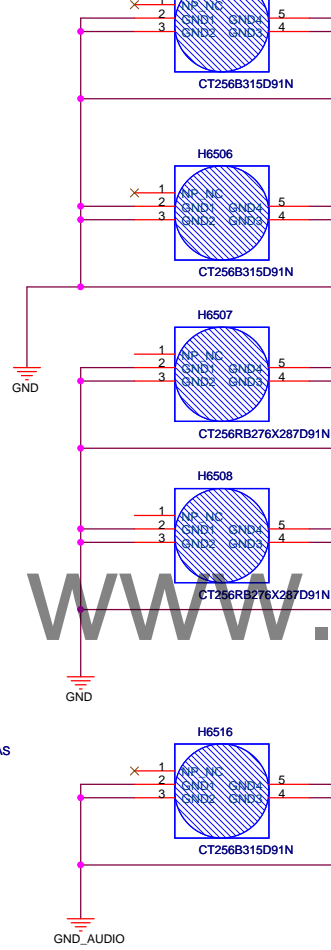
# Spring



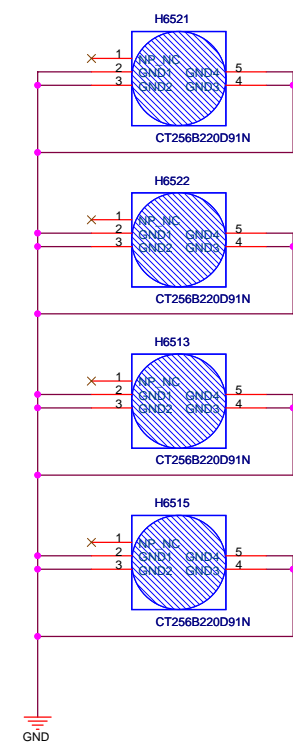
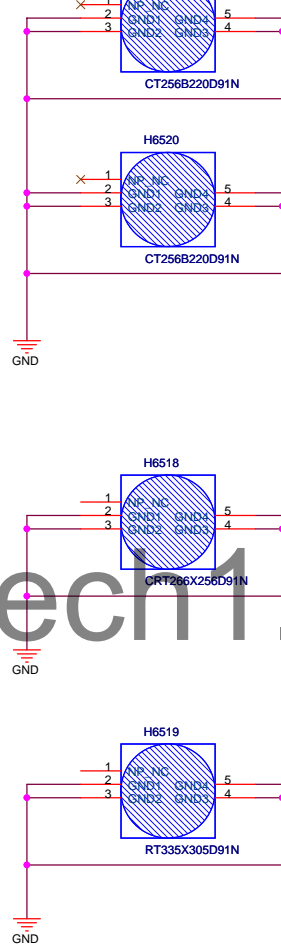
# Hole-D




# Hole-E



# Hole-F



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		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name K40AA	Rev 1.00
Date: Monday, February 09, 2009		Sheet 67 of 87

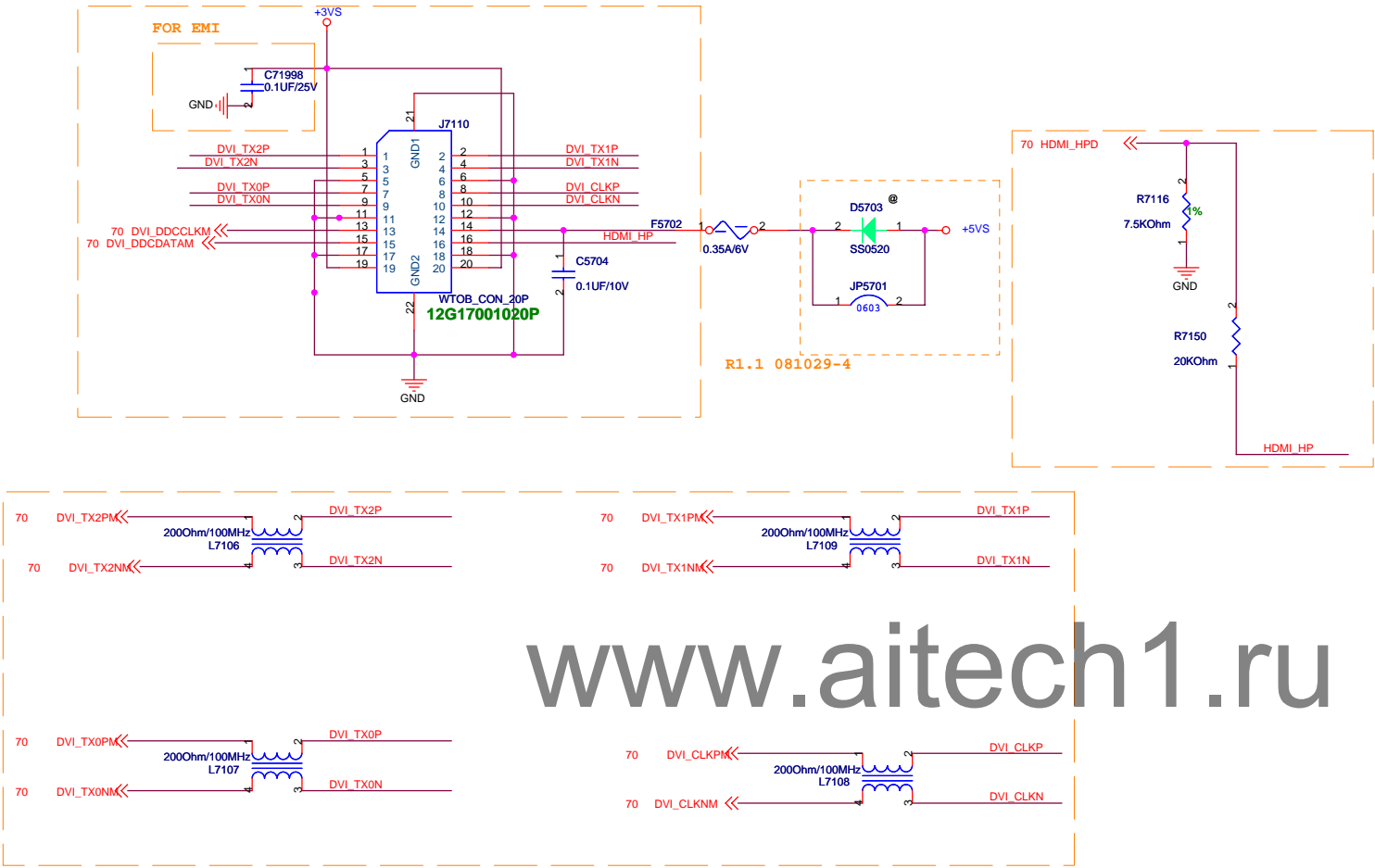
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		Title : OTH_RAID	
ASUSTeK COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name		Rev
C	K40AA		1.0
Date: Monday, February 09, 2009		Sheet	69 of 87

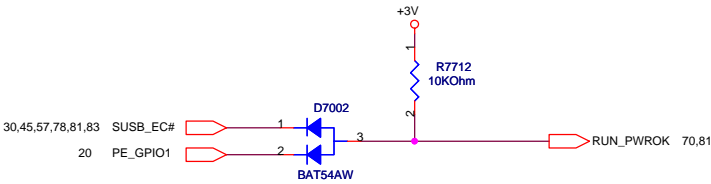


HDMI CONNECTOR

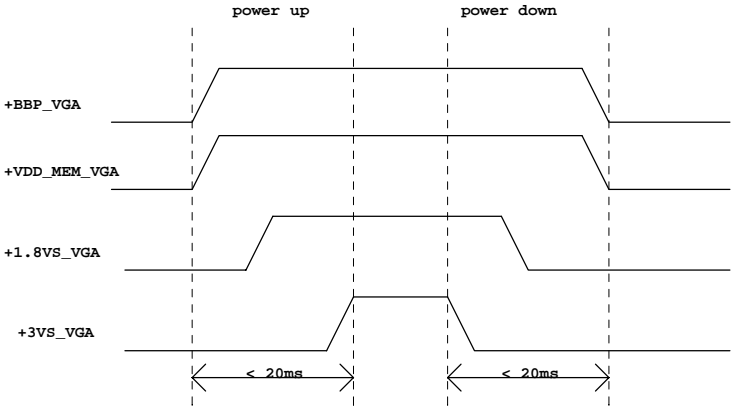


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GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V

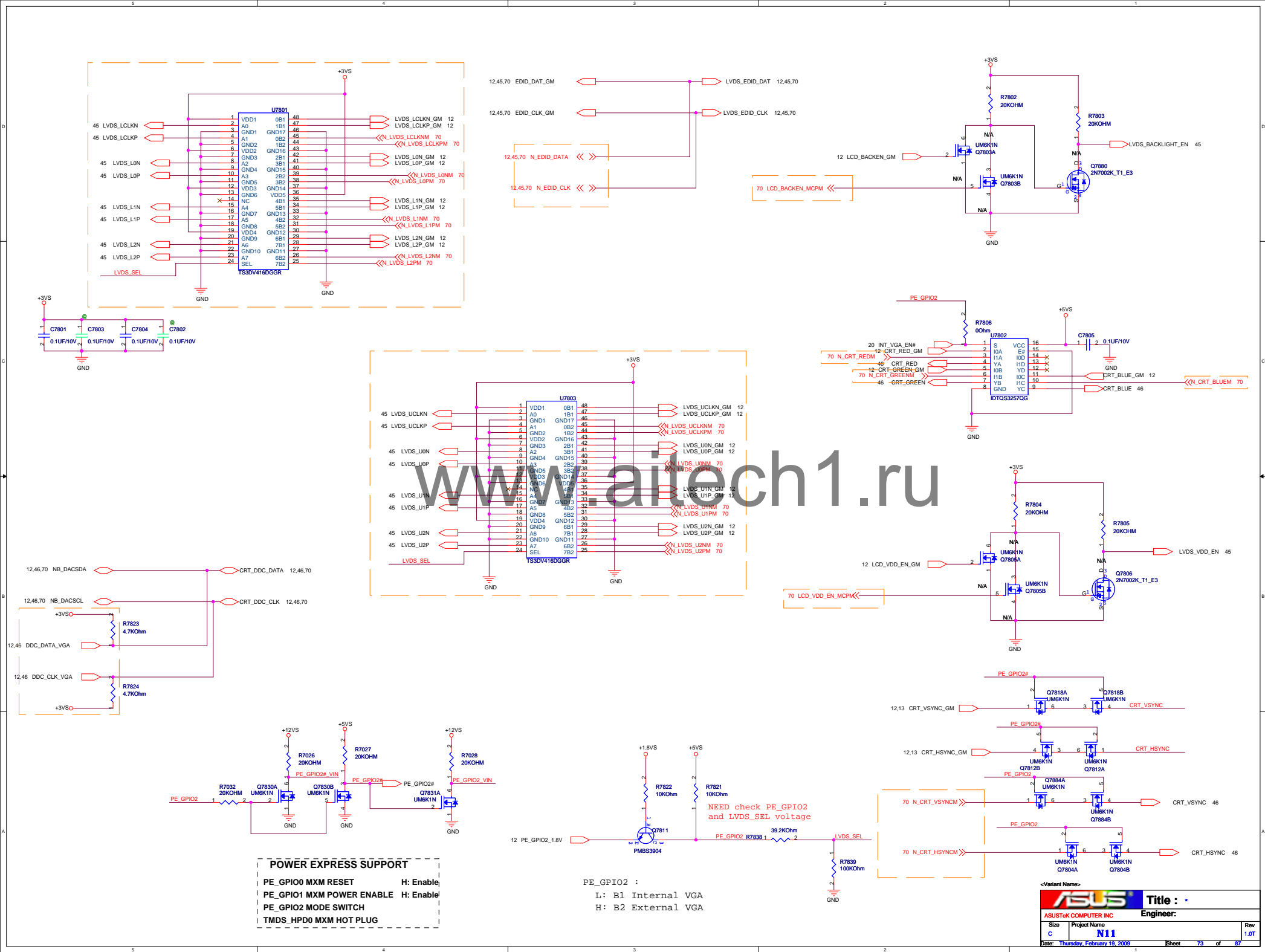


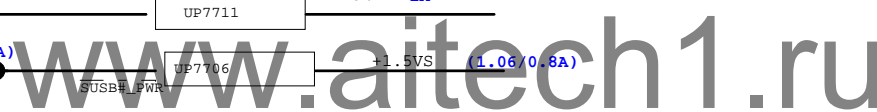
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1.1-V rails should ramp before, or together with the 1.8-V rails.  
The 1.1-V nominal voltage rails should never lag the 1.8-V nominal  
voltage rails by more than 1.1 V within a 1 ms window.

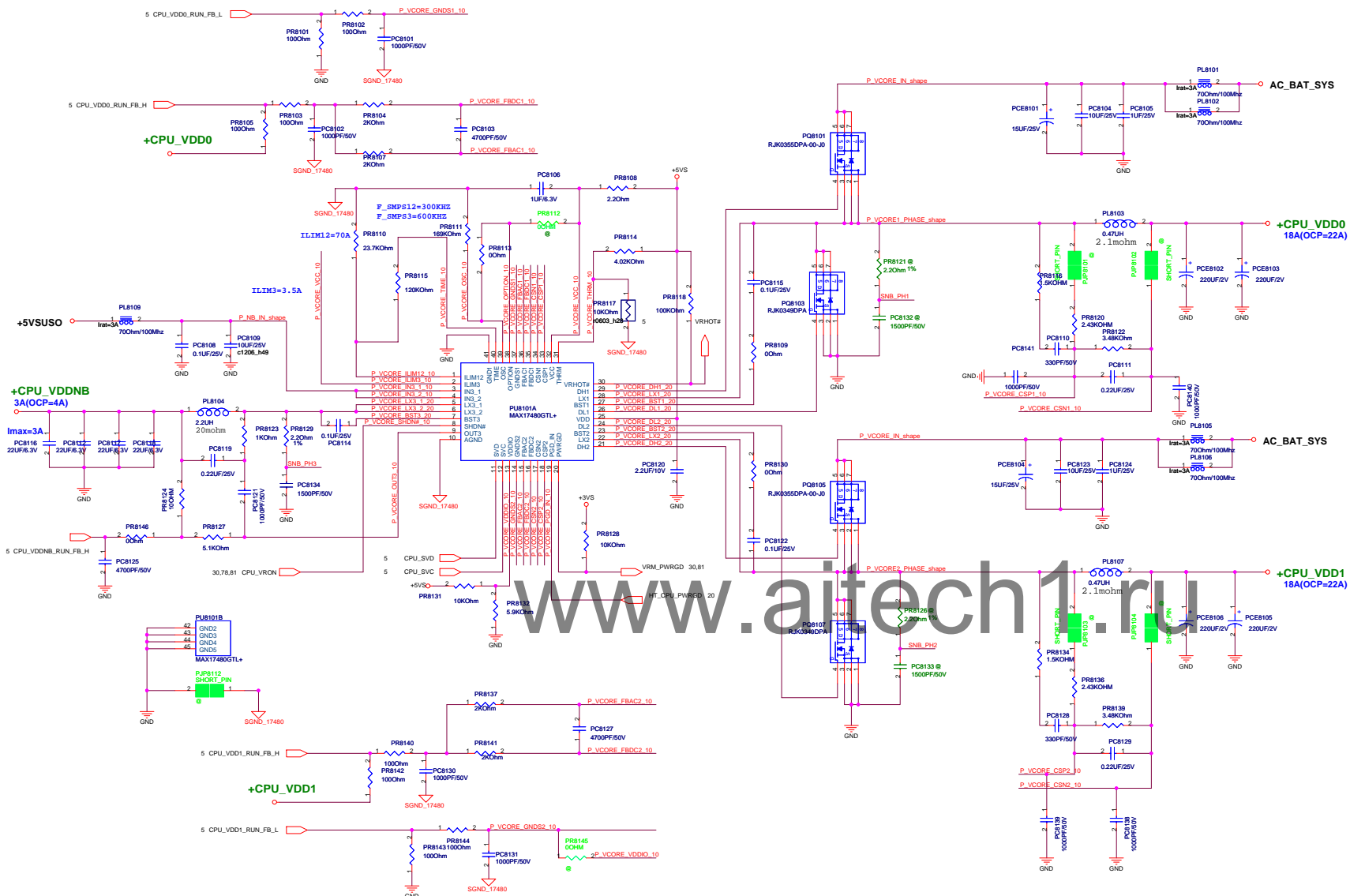


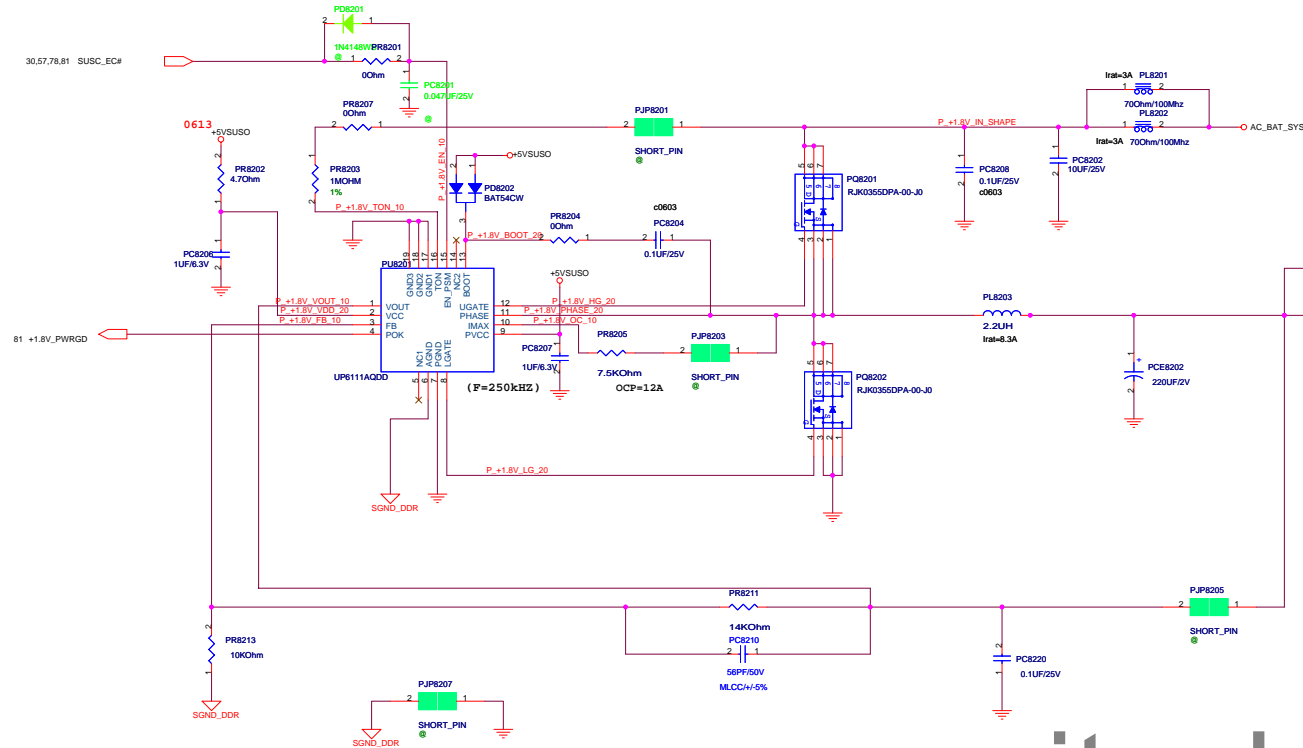




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<Variant Name>			Title : Power_FLOW	
ASUSTeK COMPUTER INC			Engineer: N/A	
Size	Project Name			Rev
A	Oemga			1.0
Date: Monday, February 09, 2009		Sheet 75 of 87		





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### Controller

#### 1. Voltage & Current:

+1.8V: 8A

#### 2. Frequency:

$T_{on} = 3.85 \mu s \cdot R_t(ON) \cdot V_{out} / (V_{in} - 0.5)$   
 $F_{frequency} = V_{out} / (V_{in} \cdot T_{on})$   
 $= 250 \text{ KHz}$

#### 3. OCP:

Set PR8205=2.15kOhm  
 $I_{OCP} = R_{OCP} \cdot 20 \mu A / R_{ds(ON)} = 12A$

#### 4. Soft start time:

Soft-Start duration is 1.35ms

#### 5. Inrush Current:

C total = 220uF  
 $I_{inrush} = 0.163A$

### Power stage

#### 1. IP Current:

$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.035A$

#### 2. Ripple Current:

Ripple=2.4A

#### 3. Dynamic:

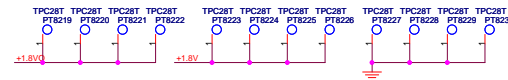
$I_{peak} = 9.5A$   
 $ESR/2 = 4.5m\Omega$   
 $V = 42.75mV$

#### 4. Inductor Spec:

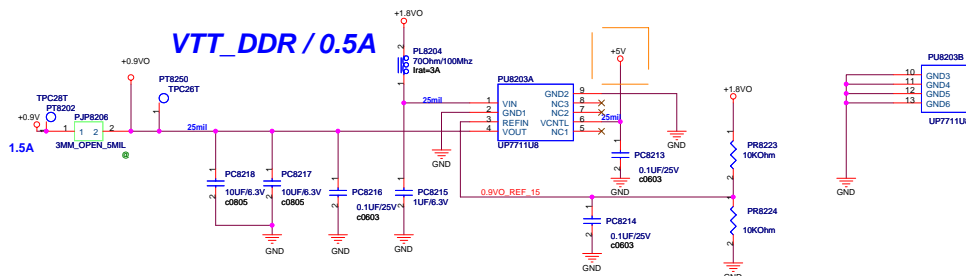
$I_{sat} = 25A$   
 $I_{dc} = 15.5A$   
 $DCR = 5.5m\Omega$

#### 5. MOSFET Spec:

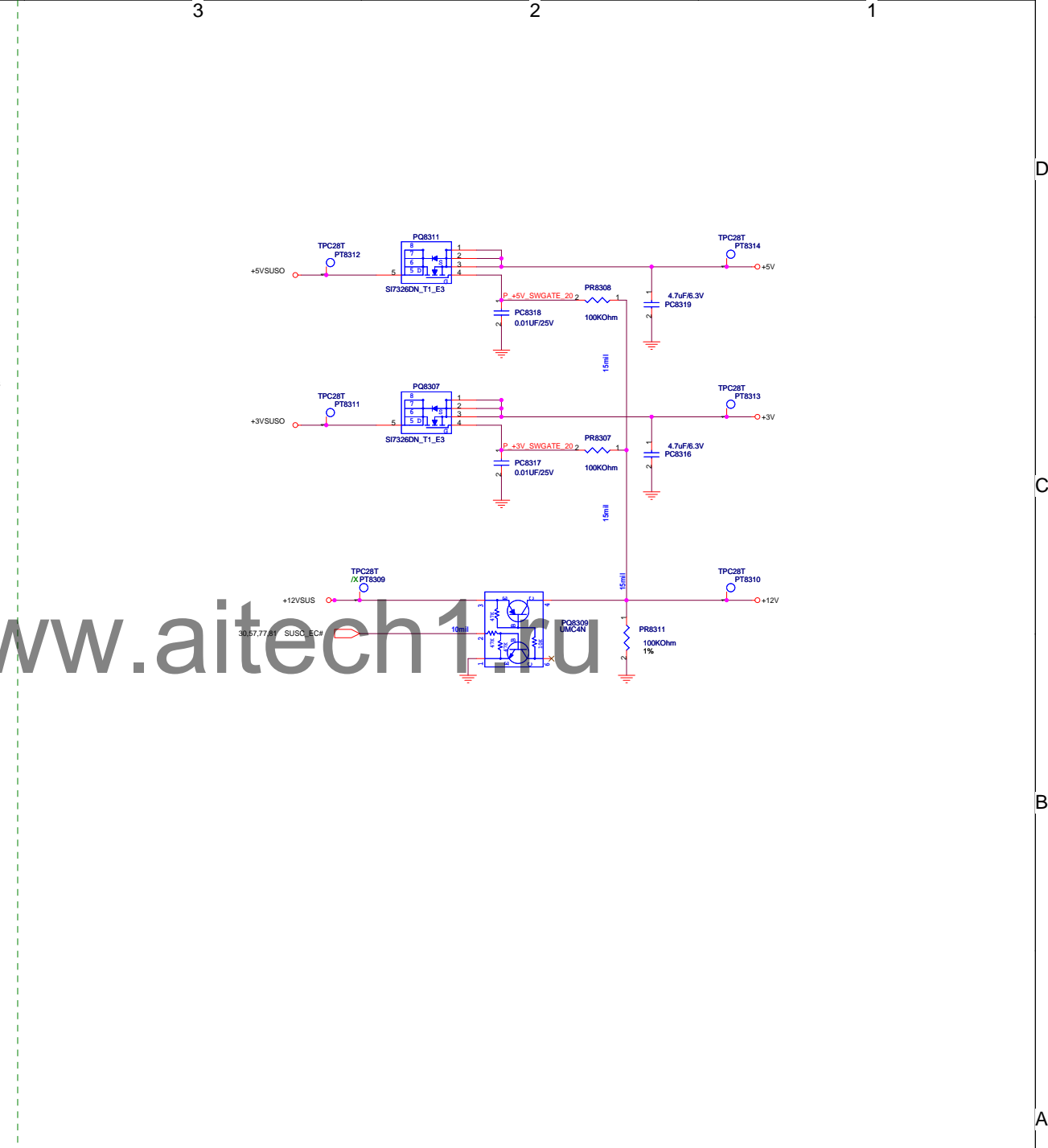
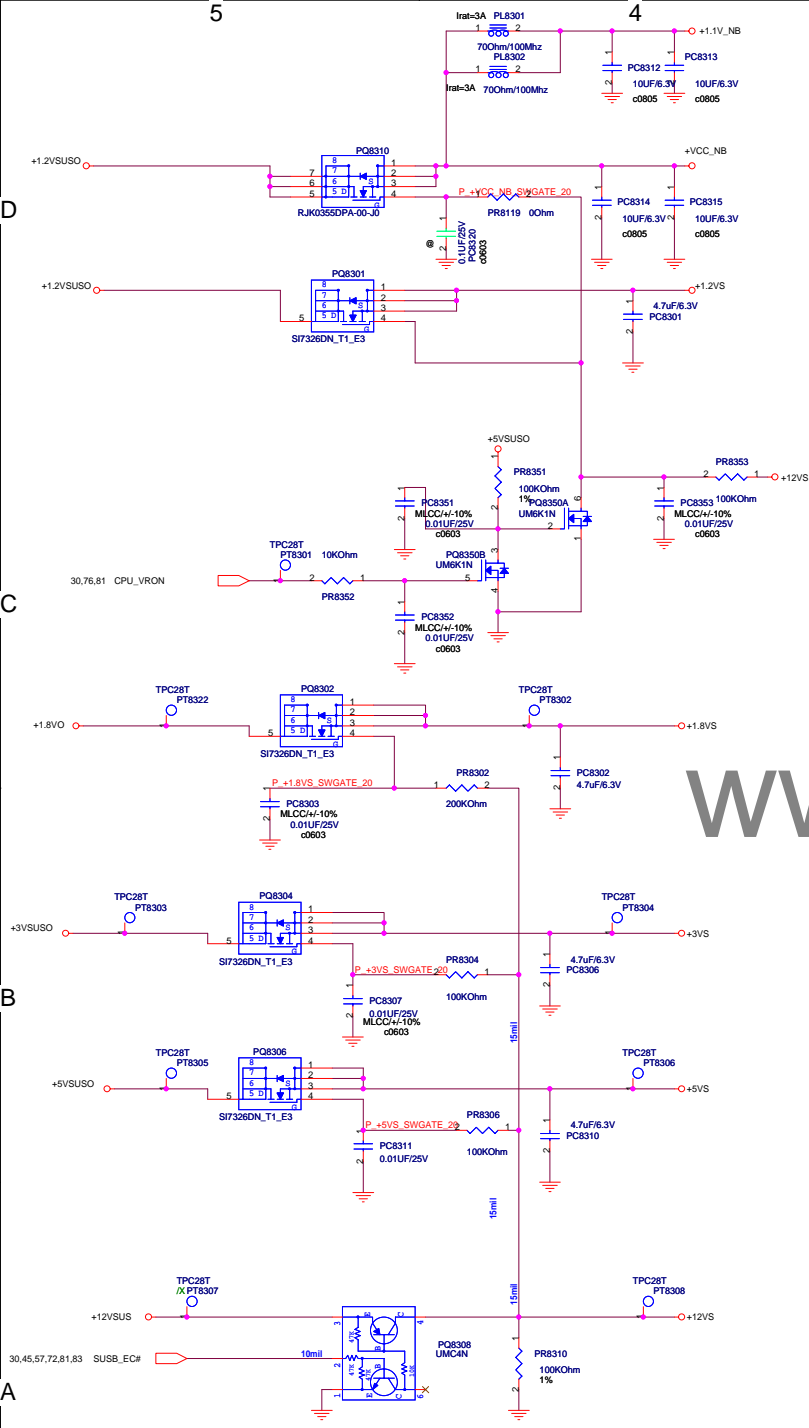
H-side and L-side MOSFET:  
 $R_{ds(ON)} = 16.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25$ )  
 $I_{peak} = 120A$  (Pause < 10us)



### VTT\_DDR / 0.5A




<Variant Name>

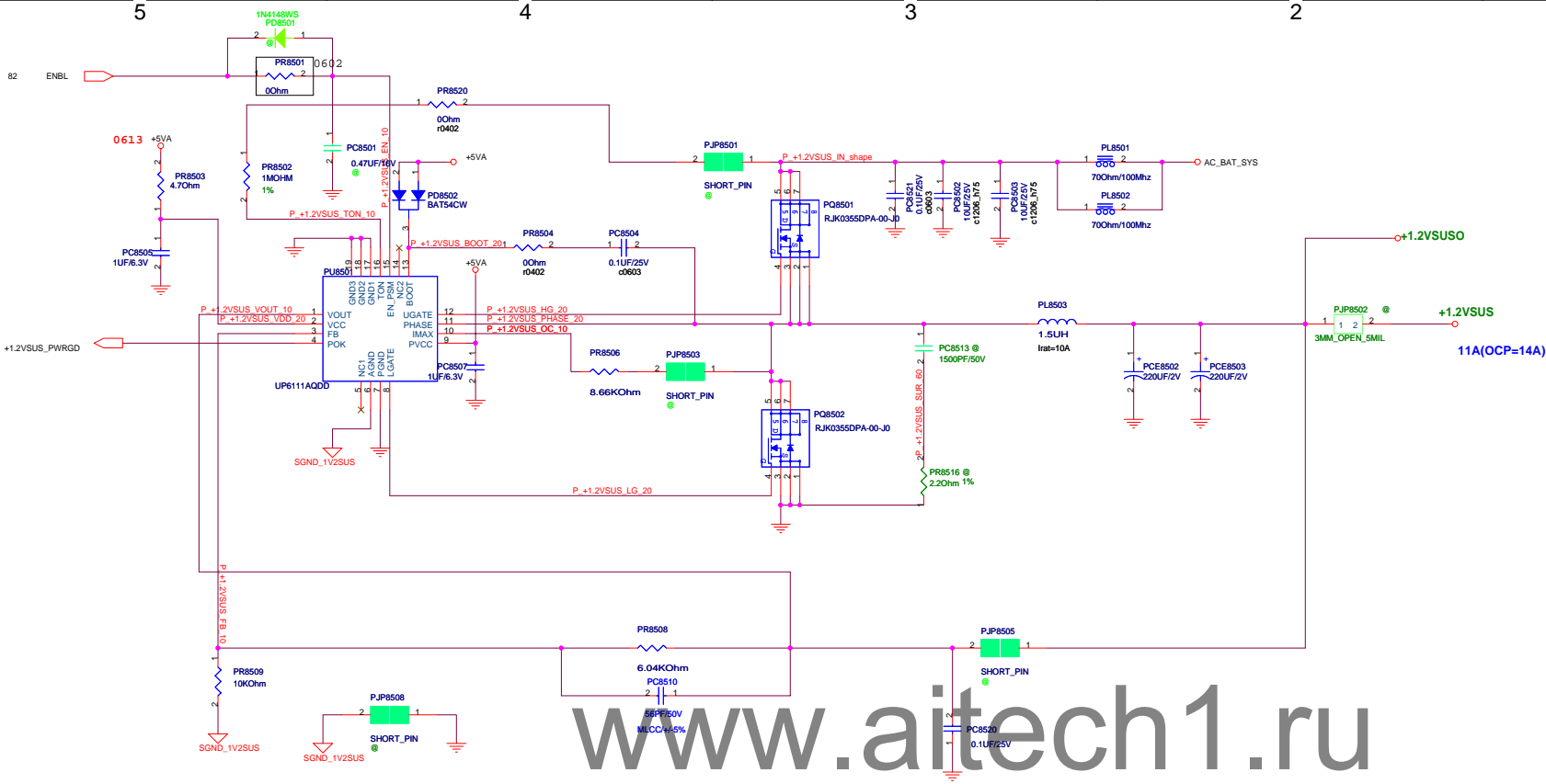


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<Variant Name>		Title : LOAD SWITCH	
ASUSTek COMPUTER INC		Engineer: <b>Sting</b>	
Size	Project Name	Oemga	Rev 1.0
Date: Thursday, February 19, 2009	Sheet	78	of 87

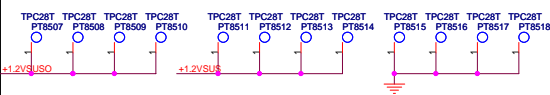
www.aitech1.ru

<Variant Name>			
		Title : Power_Charger	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
Custom			1.0
Date: Monday, February 09, 2009		Sheet	79 of 87



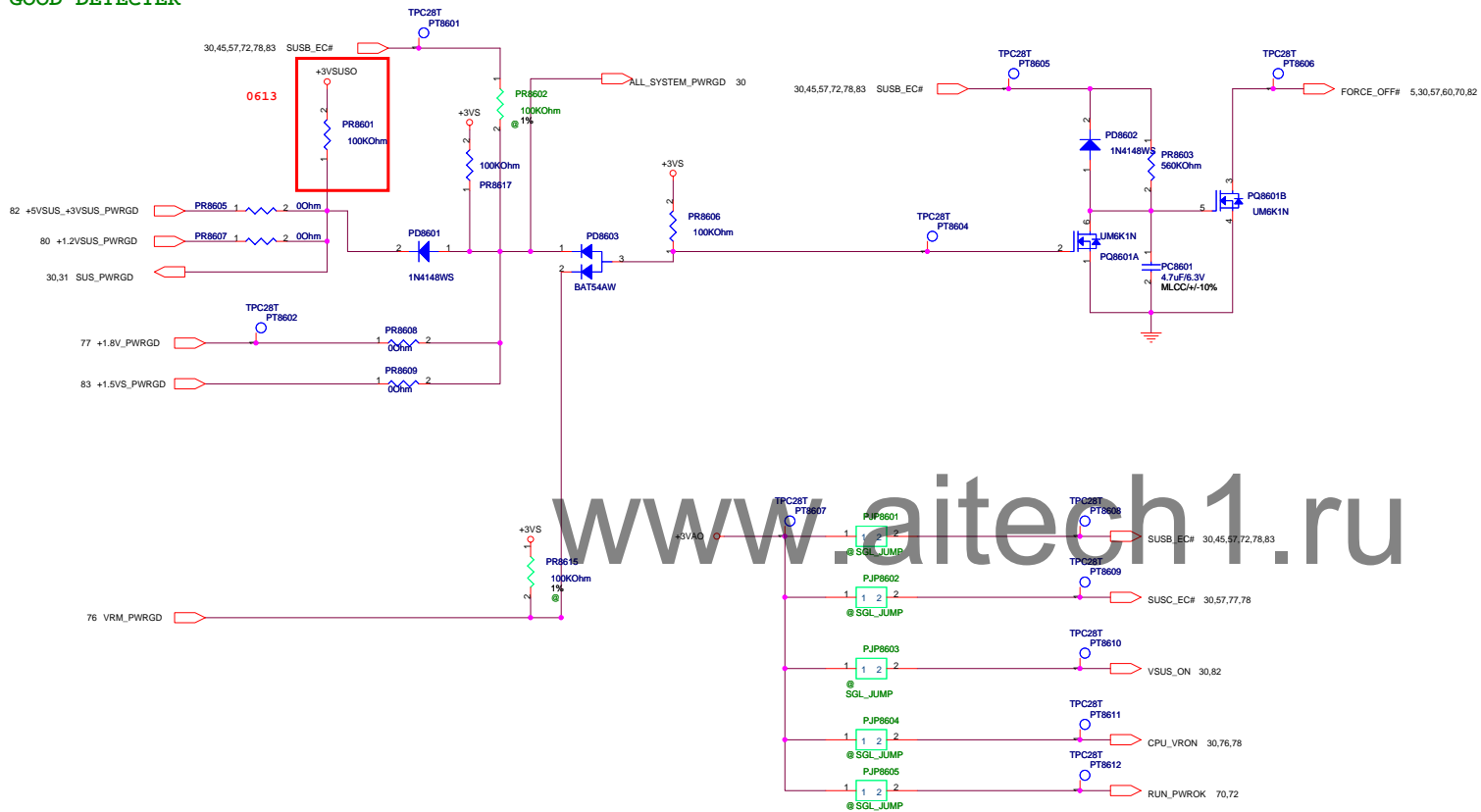
www.aitech1.ru

Controller	Power stage
<p>1. Voltage &amp; Current:</p> <p>+1.2VSUS: 11A</p> <p>2. Frequency:</p> <p>Ton=3.85p*Rt(on)*Vout/(Vin-0.5)</p> <p>Frequency=Vout/(Vin*Ton)</p> <p>=250KHZ</p> <p>3. OCP:</p> <p>Set PR8506=2.55kohm</p> <p>Iocp=Rocp*20uA/Rds(on)=14A</p> <p>4. Soft start time:</p> <p>Soft-Star duration is 1.35ms</p> <p>5. Inrush Current:</p> <p>C total =220uF</p> <p>I inrush=0.163A</p>	<p>1. I/P Current:</p> <p><math>I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.85A</math></p> <p>2. Ripple Current:</p> <p>Iripple=2.5A</p> <p>3. Dynamic:</p> <p>Ipeak=6.35</p> <p>ESR/2=4.5mohm</p> <p>V=28.575mV</p> <p>4. Inductor Spec:</p> <p>Isat=25A</p> <p>Idc=15.5A</p> <p>DCR=5.5mohm</p> <p>5. MOSFET Spec:</p> <p>H-side and L-side MOSFET:</p> <p>Rds(on)=16.5mOhm (Vgs=4.5V)</p> <p>Icont=30A (T=25)</p> <p>Ipeak=120A (Pause&lt;10us)</p>





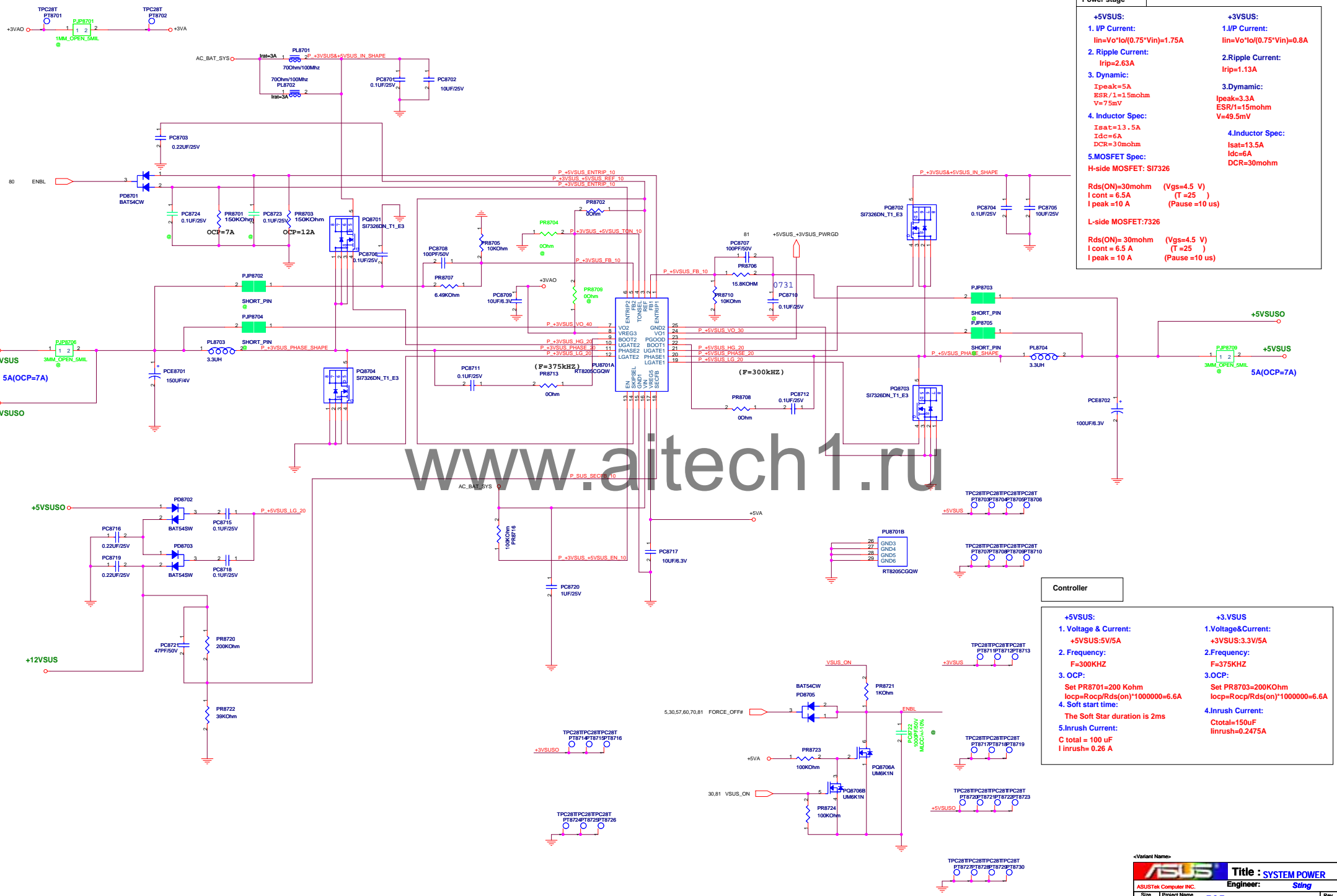
# POWER GOOD DETECTOR



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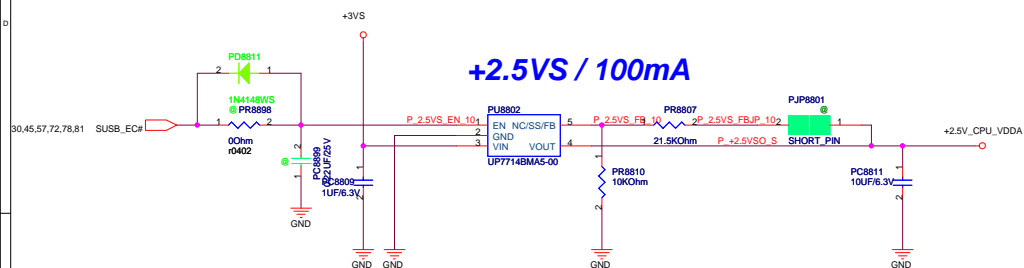
<Variant Name>

<b>ASUS</b>		<b>Title : GOOD_DETECTOR</b>	
ASUSTeK COMPUTER INC		Engineer: <i>String</i>	
Size C	Project Name K505A	Rev 1.0	
Date: Thursday, February 19, 2009		Sheet 81	of 87



Power stage	
<b>+5VSUS:</b> 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.75A$ 2. Ripple Current: $I_{rip} = 2.63A$ 3. Dynamic: $I_{peak} = 5A$ $ESR / 1 = 1.5mohm$ $V = 75mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: SI7326 $R_{ds(ON)} = 30mohm$ $I_{cont} = 6.5A$ $I_{peak} = 10A$	<b>+3VSUS:</b> 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.8A$ 2. Ripple Current: $I_{rip} = 1.13A$ 3. Dynamic: $I_{peak} = 3.3A$ $ESR / 1 = 15mohm$ $V = 49.5mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ L-side MOSFET: 7326 $R_{ds(ON)} = 30mohm$ $I_{cont} = 6.5A$ $I_{peak} = 10A$

Controller	
<b>+5VSUS:</b> 1. Voltage & Current: <b>+5VSUS: 5V/5A</b> 2. Frequency: $F = 300KHZ$ 3. OCP: Set PR8701=200 Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ The Soft Star duration is 2ms 5. Inrush Current: $C_{total} = 100 \mu F$ $I_{inrush} = 0.26A$	<b>+3VSUS:</b> 1. Voltage & Current: <b>+3VSUS: 3.3V/5A</b> 2. Frequency: $F = 375KHZ$ 3. OCP: Set PR8703=200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Inrush Current: $C_{total} = 150 \mu F$ $I_{inrush} = 0.2475A$



**2.5V @ 0.2A**

1. Dropout Voltage:

$V = 0.21V$  ( $I_o = 0.3A$ )

2. Current Limit:

$I_{limit} = 320mA$

3. Continue Current:

$I_{cont} = 300mA$

4. Power Dissipation:

$R_{thjc} = 250$  /W

$P_d = 0.4W$

5. EN Voltage:

$V_{rising} = 2V$

$V_{falling} = 0.8V$

6. Supply Voltage:

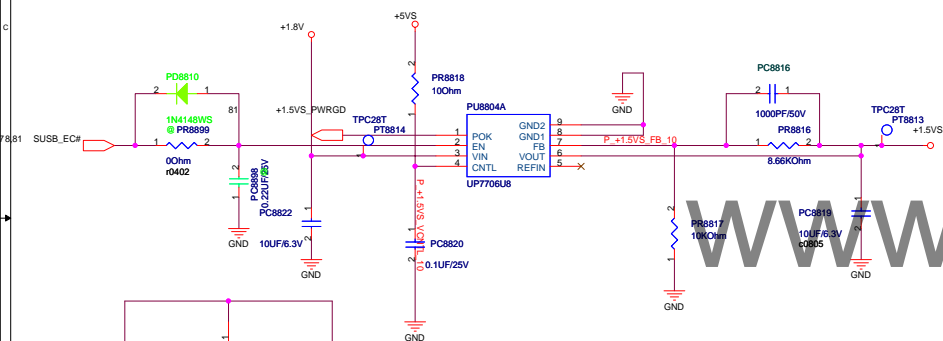
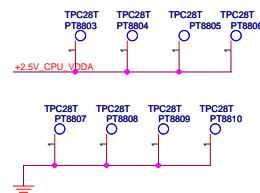
$V_{cc} = 3V$

7. Inrush current:

$T_{ss} = 400us$

$C_{total} = 10uF$

$I_{inrush} = 0.063A$



**+1.5V @ 1.2A**

1. Dropout Voltage:

$V = 0.3V$  ( $I_o = 2A$ )

2. Current Limit:

$I_{limit} = 4A$

3. Continue Current:

$I_{cont} = 2A$

4. Power Dissipation:

$R_{thjc} = 52$  /W

$P_d = 1.9W$

5. EN Voltage:

$V_{rising} = 1.4V$

$V_{falling} = 0.8V$

6. Supply Voltage:

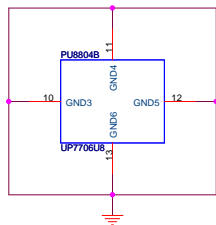
$V_{cc} = 5V$

7. Inrush current:

$T_{ss} = 400us$

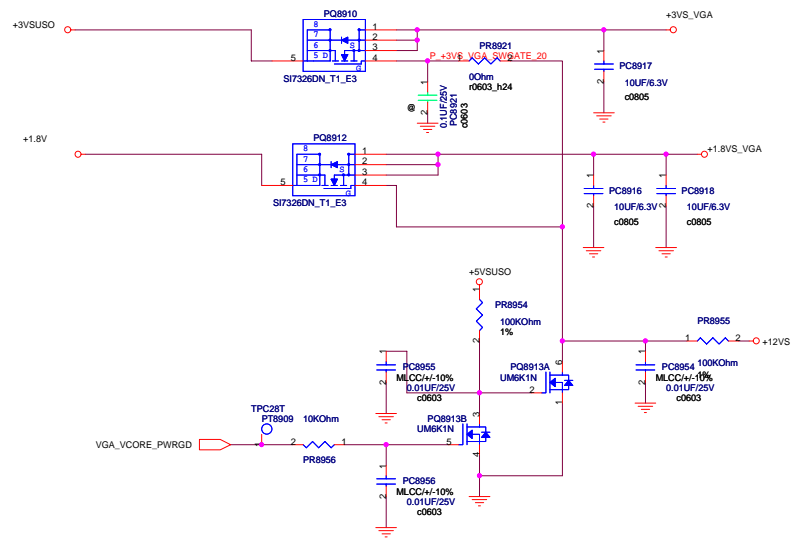
$C_{total} = 10uF$

$I_{inrush} = 0.063A$




<Variant Name>

<b>ASUS</b>		Title : +2.5V&+1.5V&+1.1V_Nb	
ASUSTek Computer INC.		Engineer: <i>Sting</i>	
Size	Project Name	K505A	Rev
C			1.0
Date: Thursday, February 18, 2009		Sheet	83 of 87

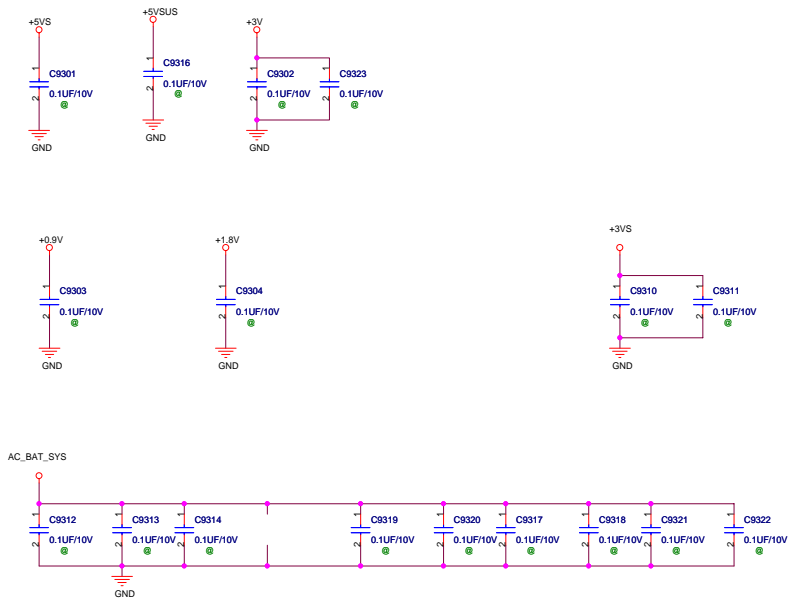


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		Title :	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
Custom	Oemga		1.0
Date: Monday, February 09, 2009		Sheet	85 of 87





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